NTAG I²C Explorer Kit user's manual

NFC communication

Near Field Communication (NFC) is a short-range, intuitive, wireless connectivity specifically designed and engineered to provide zero power operation and maximize privacy at very low cost. Because they function as wireless dual-port memories, NFC connected tags (packaged NFC devices that include a hardwired bus interface) are useful in any application that can take advantage of data transfer between an embedded system and an external reader/writer (e.g., an NFC-enabled mobile device). In fact, NFC connected tags enable exciting new capabilities for applications ranging from home automation to home appliances, health care tracking to utility monitoring, zero power electronic product configuration to zero effort consumable goods replenishment—the long touted "Internet of Things" actually come to life, but with greater privacy protection and lower cost than other approaches.

NTAG I²C connected tag chip

The NTAG I²C tag chip, the first connected product of NXP's NTAG family, offers both contactless (NFC Forum compliant) and contact (I²C serial bus) interfaces (see Figure 1). If it has an external power supply, or by using its embedded energy-harvesting feature to power itself, the NTAG I²C device can communicate with a microcontroller or other I²C-compatible device via its I²C serial bus. The NTAG I²C device contains two memory types:

- EEPROM memory compliant with the NFC Forum Type 2 Tag implementation
- 64-byte SRAM memory, which is mapped within the EEPROM memory and powered externally

Without an external power supply, the NTAG I²C tag chip can communicate via its RF interface as a passive NFC tag, and because it contains EEPROM, store data for later retrieval via the I²C serial bus. Under power, the SRAM memory supports a Pass-Through mode that allows fast download and upload of data from the RF interface to the I²C interface and vice versa without affecting the EEPROM access limitations, essentially creating a wireless RF to connected I²C serial bus bridge.

The NTAG I²C device can also use its energy-harvesting feature to supply power to external (low power) devices, such as microcontrollers, for zero external power operation. A separate, configurable Field Detection pin provides an external trigger depending on the activities at the RF interface, avoiding processor cycle consuming polling schemes, and delivering additional application flexibility.

For a brief video introduction to the NTAG I²C Explorer Kit, please visit http://nxp-rfid.com/ntag-i2c-explorerkit/ and click on "Watch Quick Start Guide Video".

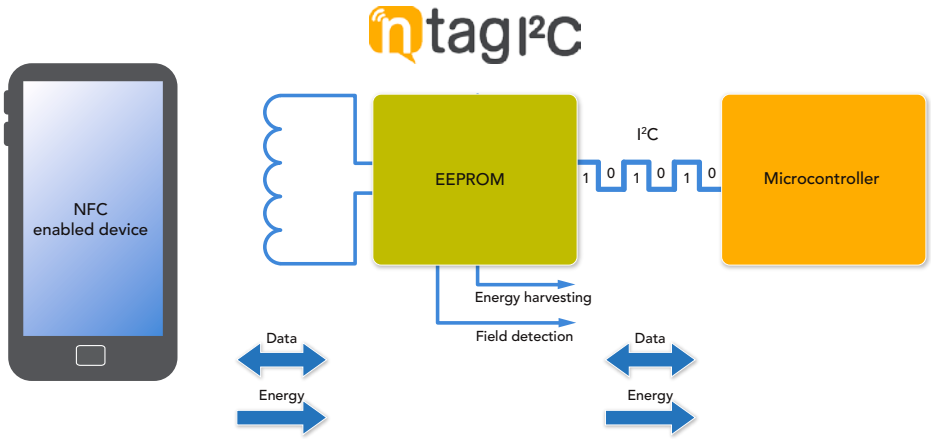


Figure 1. NTAG I²C tag chip contact and contactless interfaces

NXP offers the NTAG I²C product in two different versions: the NTAG I²C 1K version with 888 bytes freely available in the user memory, and the NTAG I²C 2K version with 1904 bytes freely available in the user memory.

NTAG I²C Explorer Kit contents

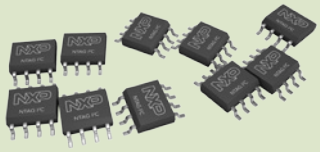
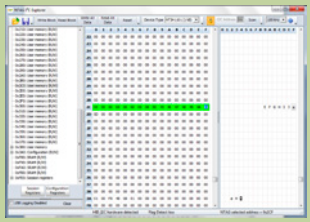
To demonstrate the unique properties of the NTAG I²C tag chip, NXP developed the NTAG I²C Explorer Kit, an all-in-one demonstration/development resource for NFC connected tag chips. By including a full complement of hardware and software tools, users can not only investigate the capabilities of the chip through the various demonstrations, but also develop and test their own applications (with purchase of the optional LPC-Link2 debug probe).

NXP's NTAG I²C Explorer Kit supports interactive demonstrations and enables exploration of all NTAG I²C tag chip capabilities for both the hardware designer and the application developer. Optionally, the addition of the LPC-Link2 Debugger probe kit allows easy debugging of code ported directly in the NTAG I²C Explorer Board, facilitating custom applications.

Table 1 NTAG I²C Explorer Kit components

NTAG I²C Explorer Board A dual purpose demonstration and development hardware board based on the NXP LPC 11U24 microcontroller, with onboard LCD display, NXP PCT2075 temperature sensor, voltage monitors, I²C serial bus connector, and JTAG/SWD debug connector to demonstrate bi-directional I²C serial bus/NFC communication, illustrate NDEF messaging, monitor energy harvesting capability, and provide a localized application development environment	
NFC Antennas NTAG I²C tag chips mounted on a variety of different antenna types (Class 4, 5, and 6 FR4 PCB-based with separate antenna pads for custom antenna use, as well as a Class 6 Flex-board based tag for easier product insertion testing) and with built-in I²C serial bus interface connectors	
NTAG I²C demo From the Google Play Store, load the Android™ application: "NTAG I2C Demoboard," an interactive demonstration application for NFC-enabled phones	

Table 1 NTAG I²C Explorer Kit components

NTAG I²C packaged samples	
Peek and Poke A PC-based NTAG I²C device register and memory exploration software tool with a graphical user interface	
NFC RF Detector Board An RF detector with visual (LED) output to facilitate location of the optimum RF field, or to ensure that NFC has been enabled	
NFC USB Reader PC-based PN544PC NFC reader using the NXP LPC11U24 microcontroller with associated graphical user interface and USB-micro to USB cable for those without an NFC-enabled mobile device, where one desires additional performance over the mobile device reader/ writer capability, or for embedded applications	
USB/micro USB cable	

Optional LPC-Link2 debug probe

The LPC-Link2 debug probe is a low-cost development tool platform for the LPC MCUs (such as the LPC 11U24) including a target board with integrated debug probe plus debug ribbon cable, and supported by an Eclipse-based integrated development environment.

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1 Definitions

1.1 Nomenclature and acronyms

For convenience sake, the following shortcut names and acronyms are used in the document:

- Explorer Board: NXP NTAG I²C Explorer Board (see Section 2.2.1.1)
- Reader Board: USB-based, PN544 NFC transceiver board (see Section 2.2.1.3)
- Peek and Poke: NTAG I²C Explorer Peek and Poke (see Section 2.2.2)

1.2 Antenna classes defined

The ISO/IEC standard describes six antenna classes (Class 1 through Class 6), which refer to their form factor and size. For an NFC tag, NXP recommends using "Class 3" through "Class 6." The following describes these recommended form factors/sizes. For more information, see the NTAG Antenna Design Guide Application Note (AN11276).

1.2.1 "Class 3" antennas

A "Class 3" antenna shall meet the requirements of being located within a zone defined as (see Figure 1-1):

- An external rectangle of 50 x 40 mm
- An internal rectangle of 35 x 24 mm, centered in the external rectangle, with 3 mm corner radii

OR

- An external circle with diameter of 50 mm
- An internal circle with diameter of 32 mm, concentric with the external circle

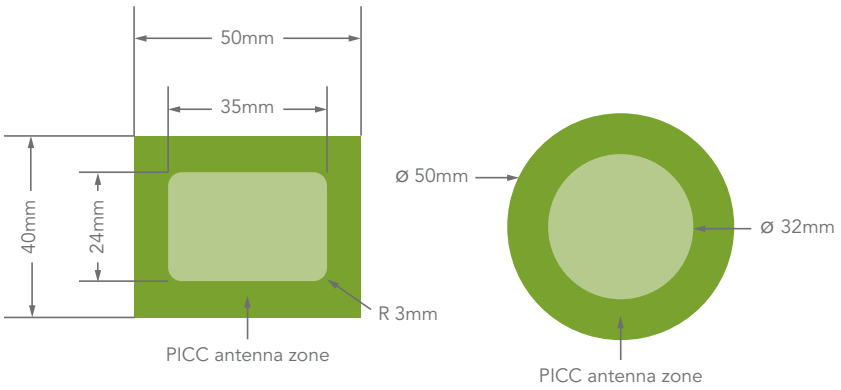

Figure 1-1. "Class 3" antenna specified zones

1.2.2 "Class 4" antennas

A "Class 4" antenna shall meet the requirements of being located within a zone defined as (see Figure 1-2):

- An external rectangle of 50 x 27 mm
- An internal rectangle of 35 x 13 mm, centered in the external rectangle, with 3 mm corner radii

OR

- An external circle with diameter of 41 mm
- An internal circle with diameter of 24 mm, concentric with the external circle

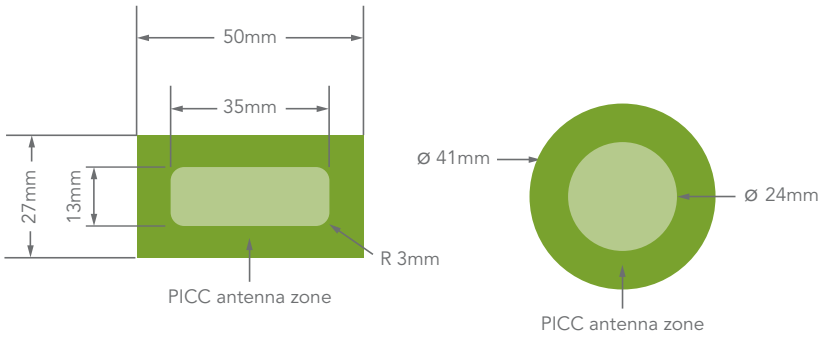

Figure 1-2. "Class 4" antenna specified zones

1.2.3 "Class 5" antennas

A "Class 5" antenna shall meet the requirements of being located within a zone defined as (see Figure 1-3):

- An external rectangle of 40.5 x 24.5 mm
- An internal rectangle of 25 x 10 mm, centered in the external rectangle, with 3 mm corner radii

OR

- An external circle with diameter of 35 mm
- An internal circle with diameter of 18 mm, concentric with the external circle

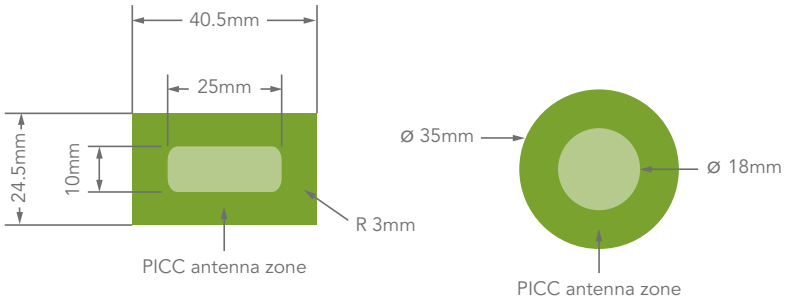

Figure 1-3. "Class 5" antenna specified zones

1.2.4 "Class 6" antennas

A "Class 6" antenna shall meet the requirements of being located within a zone defined as either a rectangle of dimensions 25 x 20 mm, or a circle of 25 mm diameter (see Figure 1-4).

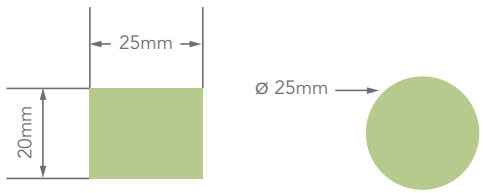

Figure 1-4. "Class 6" antenna specified zones

2 NXP NTAG I²C Explorer Kit Overview, Contents, and Setup

2.1 NTAG I²C Explorer Kit Overview

NXP developed the NTAG I²C Explorer Kit to demonstrate the operation of the NXP NTAG I²C device, and to show how it can be used in a typical energy harvesting application. The primary components of the demonstration are the Explorer Board and the NTAG I²C Antenna board, of which a variety are included (see Table 1)

The NTAG I²C Antenna board consists of an NTAG I²C tag chip assembled on a PCB connected to an antenna etched from the copper on the PCB (see NTAG I²C Antenna Board in Figure 2-1). The antenna board connects to the NXP LPC11U24 (Cortex-M0) microcontroller-based, NTAG I²C Explorer board (see Explorer Board in Figure 2-1), which receives its power from the antenna board.

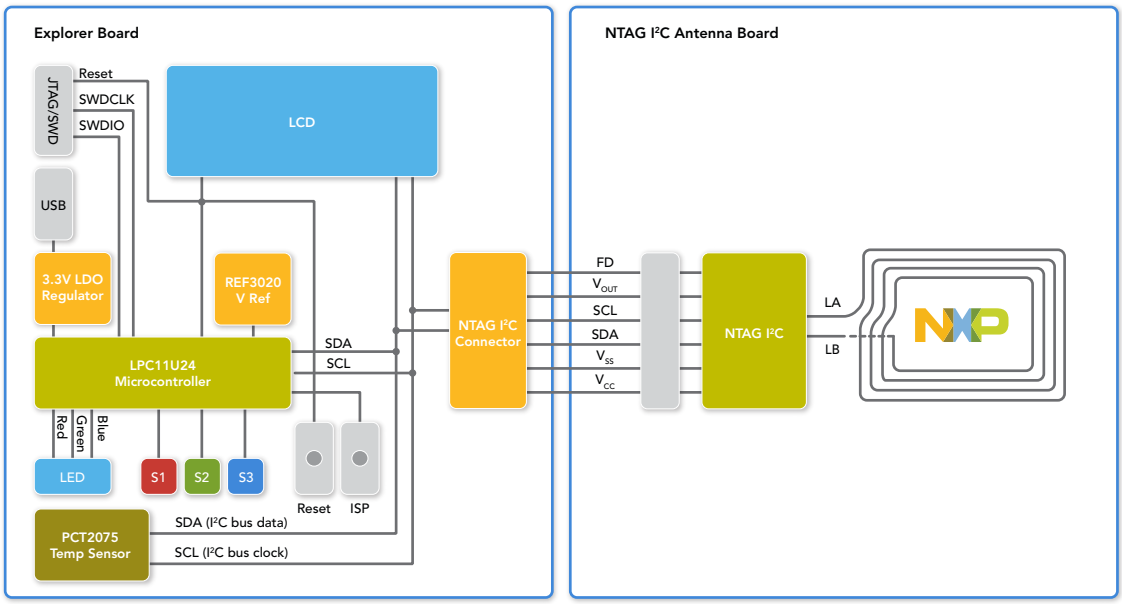

Figure 2-1. NTAG I²C Explorer Kit microprocessor and Antenna Boards

As shown in Figure 2-1, the Explorer board also hosts a 2x16 character LCD, an NXP PCT2075 temperature sensor, a voltage reference, and RGB LEDs. Because the NTAG I²C Antenna board provides power for all these parts, they must all use minimal current, while operating at voltage levels typically in the 2.7 V to 3.0 V range. Keeping the total current consumption below 5 mA is critical, because the current consumption of the development board affects the output voltage of the NTAG I²C device. If the required current is too high, the output voltage will be too low to power the board.

Although most components on the board operate down to 1.8 V, the LCD requires a minimum of 2.7 V, so this part determines the minimum voltage required by the kit. Each LED in the RGB array consumes less than 1 mA; the PCT2075 temperature sensor typically consumes less than 1 µA, because it is normally in idle mode; the LCD consumes a maximum of 0.5 mA; the microcontroller consumes approximately 1.6 mA in active mode (using an internal RC oscillator); the voltage reference typically consumes 42 µA.

The microcontroller serves as the I²C master. It acquires the temp (in °C) from the temperature sensor, and provides it via the I²C bus to the NTAG I²C device's SRAM memory buffer (in pass through mode), which passes it along in a standard NDEF formatted package via the RF interface to an NFC-enabled mobile device. The mobile device

calculates the °F conversion, and passes it back to the microcontroller, which then sends it to the LCD, also via the I²C bus. The polling rate of the Android application (see Appendix B) determines the sampling rate for this operation. Although NXP used a temperature sensor to demonstrate the RF to I²C data bridging, any low-power I²C compatible device could be used instead. One example would be to add additional memory with an I²C bus compatible memory device.

The voltage reading displayed on both the LCD and on the NFC-enabled phone GUI is representative of V_{OUT}—the voltage harvested by the NTAG I²C device from the RF field. (For more information about power harvested versus RF field strength, see the FAQs located at http://nxp-rfid.com/ntag-i2c-design-resources/). The V_{OUT} measurement is also passed along from the Explorer board to the mobile device via the SRAM memory.

The LCD has a backlight, but it is not activated unless the USB is connected, and not during conventional power harvesting mode. However, if desired, the backlight may be used if one depresses the blue switch on the Explorer board while connecting power via the USB connection. Depressing the blue button prior to insertion of the USB instructs the microcontroller to remain in the default demonstration routine. In this mode, the LCD displays "NTAGI2C Explorer." If the USB is connected without depressing the blue switch, the 5 V from the USB signals the microcontroller to switch to Peek and Poke mode. This 5v supply is passed through a 3.3 V regulator and is "or'd" with the power harvested (V_{OUT}) from the NTAG I²C device.

The Explorer board also includes a JTAG/SWD debug connector (allowing a user to create their own custom application), and a USB connector to implement a USB-I²C interface (allowing the user to review and change the contents of the internal SRAM and EEPROM in the NTAG I²C device via the Peek and Poke software provided).

The NDEF tabulation of the demonstration allows users to write and read simple text, URI or BT pair messages to and from the NTAG I²C 's EEPROM memory. The Speed tabulation of the demonstration allows one to monitor the uplink and downlink transfer rates, in Bytes/sec, as data is passed to/from either EEPROM or SRAM memory in a variety of settings, such as data length, fast mode or polling mode. This speed is limited on the RF side by the NFC protocol RF link speed of 106 kb/sec and on the I²C side by the specified bus transfer rate, which may be set to either normal (100 kb/s) or fast mode (400 kb/s).

In this mode, the 64Byte SRAM buffer is used to pass along data, and transfer rates will be affected by the efficiency of the handshaking routines, coupling link optimization (for higher voltages and strong data links), etc.

The Config tab of the demo provides users with the opportunity to reset the tag to factory configurations, read from or write to the configuration registers to set up the NTAG I²C device as desired, and read the tag memory or the status registers.

NXP included various antenna geometries, from a Class 6 sized geometry (smallest in this kit) to a Class 4 sized geometry (largest in this kit). Under normal circumstances, the larger the antenna, the better the coupling and hence the greater the harvested power. But the coupling is critical, so if the source antenna (the reader) is small, then sometimes using the smaller tag antenna couples more energy. (Ideally the reader antenna is close to the same size as the tag antenna). An NFC RF detector board is provided to help the user determine if the NFC function on their NFC phone is enabled and to identify the optimal antenna coupling location.

For users without an NFC enabled phone, the Advanced kit includes a reader board where the same type of GUI as on the mobile app may be implemented on a PC.

The development kit provides a great way to explore and demonstrate the dual access memory of the NTAG I²C and is a useful tool for the software and hardware engineer alike.

2.2 Kit contents

The NXP NTAG I²C Explorer is a hardware/software tool developers can use to understand the NXP NTAG I²C tag chip functionality and demonstrate its potential for other applications. The kit includes:

Table 2-1. NTAG I²C Advanced Explorer Kit contents

	Reference	Included	Optional purchase
NTAG I²C Explorer development/demo board with Class 4 antenna	2.1.1.1	✔	
Additional interchangeable NTAG I²C antennas (PCB and flex)	2.1.1.2	✔	
Android™ mobile app downloadable from Google Playstore	3	✔	
Peek & Poke PC-based utility to probe NTAG I²C memory map	4	✔	
NTAG I²C sample ICs	—	✔	
NFC USB Reader with PC user interface	2.1.1.3	✔	
NFC RF detector board	2.1.1.4	✔	
USB/micro-USB communication cable	2.1.1.5	✔	
Windows™ based GUI app for users without an NFC mobile device		✔	
Optional LPC-LINK2 debug probe plus debug ribbon cable	2.1.1.6		✔

2.2.1 Kit hardware

2.2.1.1 Explorer board

NXP NTAG I²C Explorer board (LCD mounted above a small PCB populated with an NXP LPC11U24 microprocessor, NTAG I²C tag chip interface connector, JTAG/SWD debug connector, RGB LED, NXP PCT2075 temperature sensor, micro USB connector, and five push button controls).

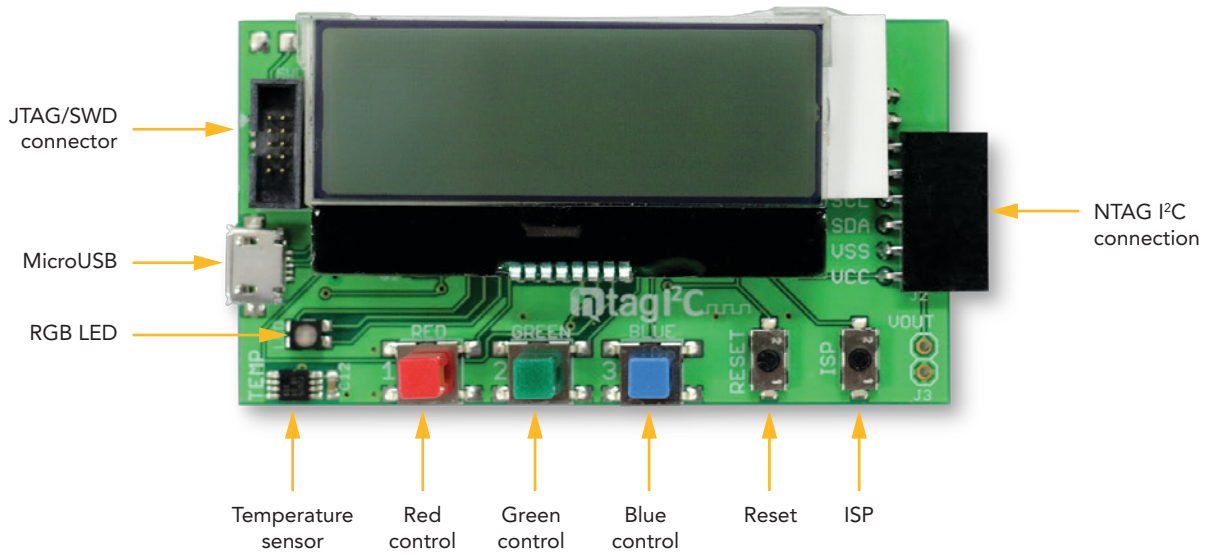

Figure 2-2. Explorer Board components

2.2.1.2 NFC antennas

NXP provides four different antenna boards (Class 4, Class 5, and two Class 6 options), so as to provide maximum flexibility and optimal coupling choices.

Note: when connecting any of the antenna boards to the Explorer board, make sure that the NTAG I²C logos (on the selected antenna board and the Explorer board) are both upright and facing you. This orientation will ensure proper pin-to-pin connection.

Class 4 antenna: Class 4 FR4 antenna board — NTAG I²C integrated circuit (IC) mounted with a Class 4 NFC antenna and a connector for the NTAG I²C IC connections of:

- FD: Field Detect
- V_{OUT}: Power harvesting output
- SCL: I²C bus clock line
- SDA: I²C bus data line
- V_{SS}: Ground
- V_{CC}: Power

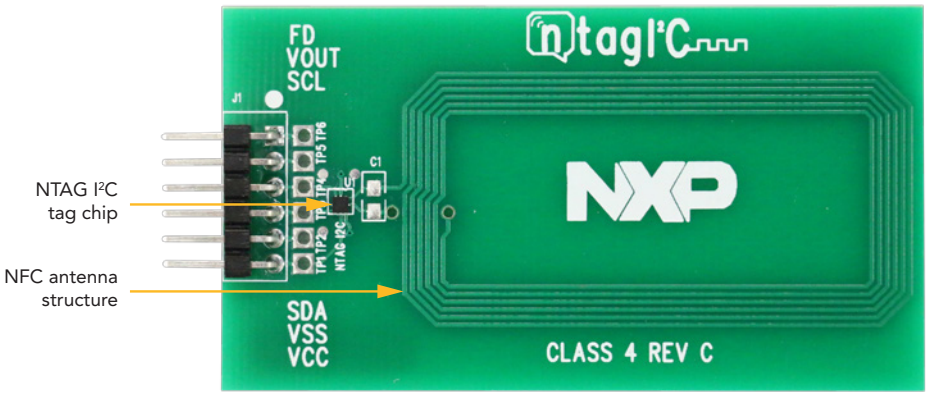

Figure 2-3. Class 4 antenna board

Class 5 antenna: Class 5 FR4 antenna board (same as Class 4 board, except with a Class 5 antenna structure). Note also the additional connection pads near the NTAG I²C chip. These pads may be used to connect a custom antenna, if desired, by cutting the traces to the on-board antenna structure, and replacing with a custom coil structure. Where C1 is not populated (see Figure 2-4), add a custom capacitor to adjust tuning or add to/replace existing capacitor on populated boards (see Figure 2-5)

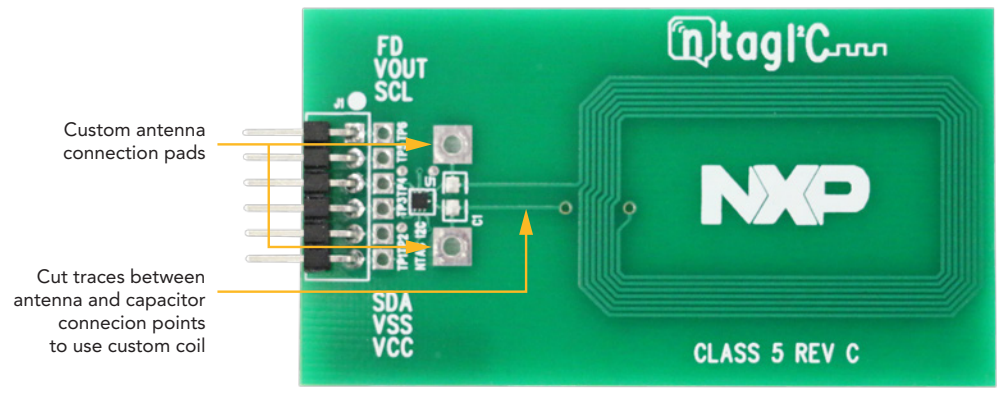

Figure 2-4. Class 5 antenna board

Class 6 Antenna: Class 6 FR4 antenna board (same as Class 4 board, except with a Class 6 antenna structure).

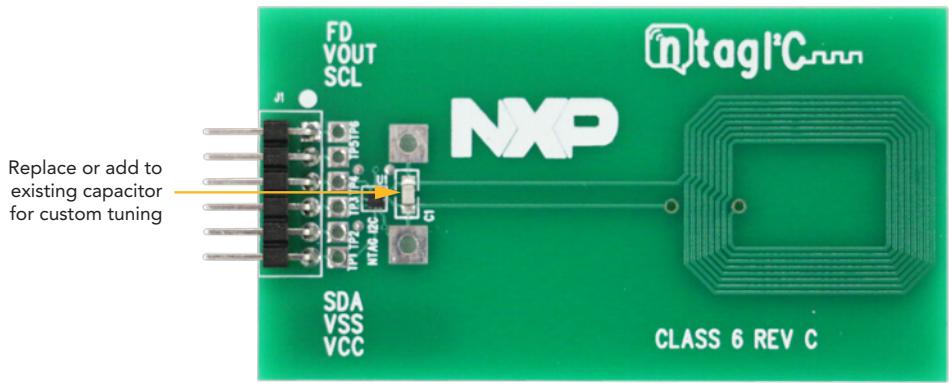

Figure 2-5. Class 6 antenna board

Flex Class 6 antenna: Class 6 flex board (same architecture as Class 6 board, except mounted on flex material and with extended traces to the connector, so that it can be inserted into products more easily).

Figure 2-6. Class 6 flex antenna

2.2.1.3 NFC USB Reader board

USB-based, PN544 NFC transceiver board controlled by an NXP LPC11U24 microprocessor to enable using a PC for the NFC tag read/write functionality

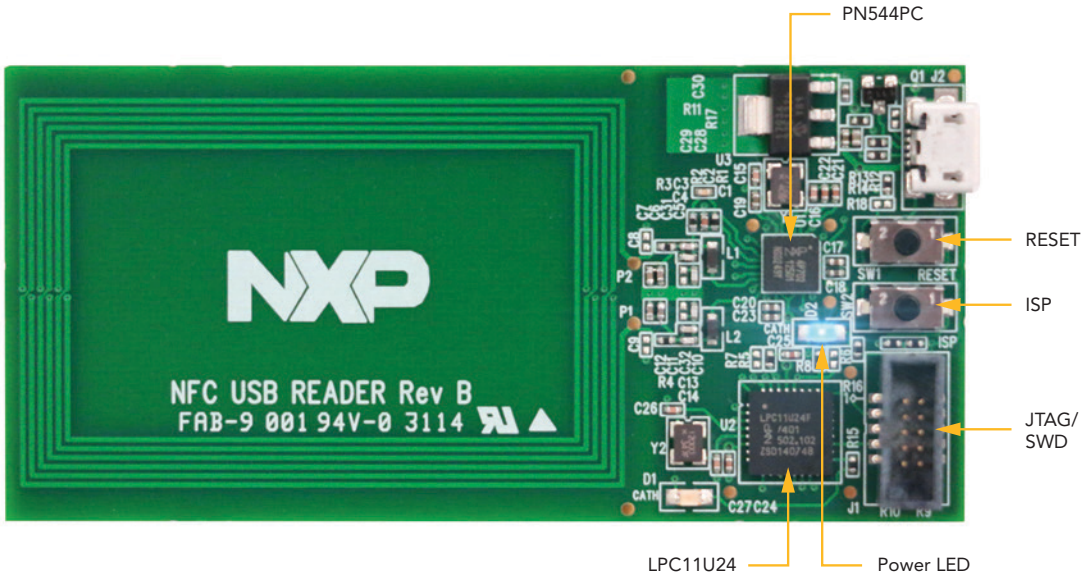

Figure 2-7. PN544 NFC transceiver board

2.2.1.4 NFC RF detector board

An RF detector with visual (LED) output to facilitate location of the optimum RF field, or to ensure that NFC has been enabled.

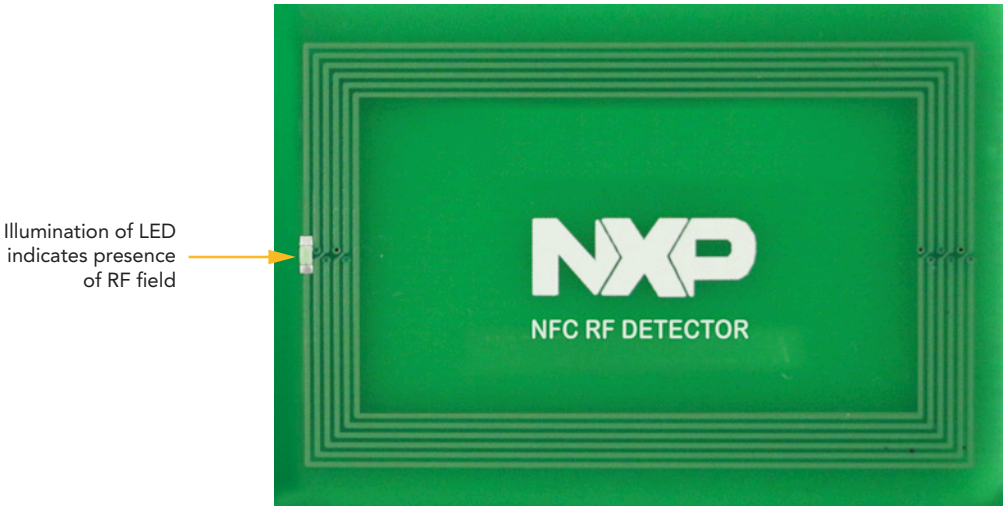

Figure 2-8. NFC RF detector board

2.2.1.5 USB to micro USB cable

Cable to use with the NTAG I²C Explorer board when using supporting "Peek and Poke" software (see Section 2.2.2), or to use with the transceiver board for the simulated mobile device graphical user interface.

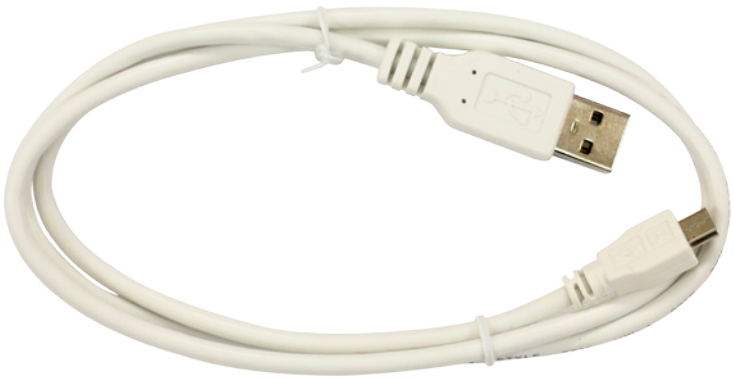

Figure 2-9. USB to micro USB cable

2.2.1.6 LPC-Link2 debug probe

An optional low-cost development tool platform for the LPC MCUs (such as the LPC 11U24) including a target board (see Figure 2-10) with integrated debug probe plus debug ribbon cable (see Section 2.3.3 and Section 6).

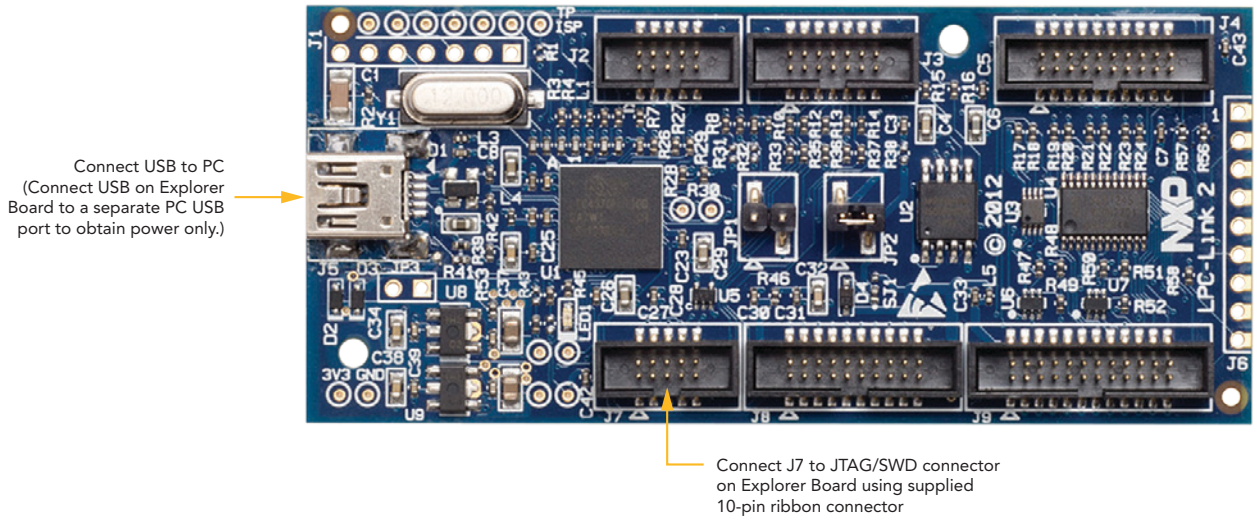
Connect USB to PC
(Connect USB on Explorer
Board to a separate PC USB
port to obtain power only.)
Connect J7 to JTAG/SWD connector
on Explorer Board using supplied
10-pin ribbon connector

Figure 2-10. LPC-Link2 debug board

2.2.2 Kit software

Supporting software also comes with the NTAG I²C Explorer Kit. This software consists of the following components:

- NTAG I²C Demoboard: An Android™ mobile phone application to enable use of an NFC-enabled mobile phone as an NFC transceiver for the demonstration/development kit. The Android application is intended to operate on devices running Android version 4.0 and beyond. The application has been optimized for a correct visioning of the graphical elements in smartphones featuring different resolutions, and is available from the Google Play Store.
- NTAG I²C Demo GUI: A PC-based GUI application to emulate the Android phone screen for users of the NFC USB Reader board.
- NTAG I²C Explorer Board Firmware: Firmware for the NTAG I²C Explorer board microprocessor, which supports the demonstration functionality of the hardware.
- NTAG I²C Explorer Peek and Poke GUI: The Peek and Poke software enables users to examine and control NTAG I²C memory and register contents, which is useful in verifying proper operation of either PC board based software or NFC reader firmware which must communicate through the chip.

2.3 System requirements and setup

This section explores NFC phone compatibility, minimal PC requirements for the Peek and Poke software to work correctly, hardware setup connections, enabling NFC operation on your Android device, load the NTAG I²C Demoboard application on your mobile device, and updating firmware on the Explorer board if necessary.

Before beginning, it might be helpful to view the "Quick Start Guide Video", available at http://nxp-rfid.com/ntag-i2c-explorerkit/

2.3.1 NFC phone compatibility

The demo application is intended to operate on devices running Android version 4.0 and beyond, and has been tested and confirmed to perform well with Google Android reference devices. Performance with various phones varies from one make and model to another as several factors impact performance, such as the size and power output of the NFC mobile device's antenna, and how the phone's operating system handles the NFC stack with different revisions of Android.

2.3.2 Minimal PC requirements

- The NTAG I²C Explorer Peek and Poke software requires an IBM® PC compatible computer running a 32-bit or 64-bit Windows® operating system (XP through Windows 8 compatible).

2.3.3 Hardware connections

The Explorer kit is highly flexible and thus has a few different hardware setups. These setups are detailed here.

Figure 2-11. Explorer Board to PC connection for firmware updates

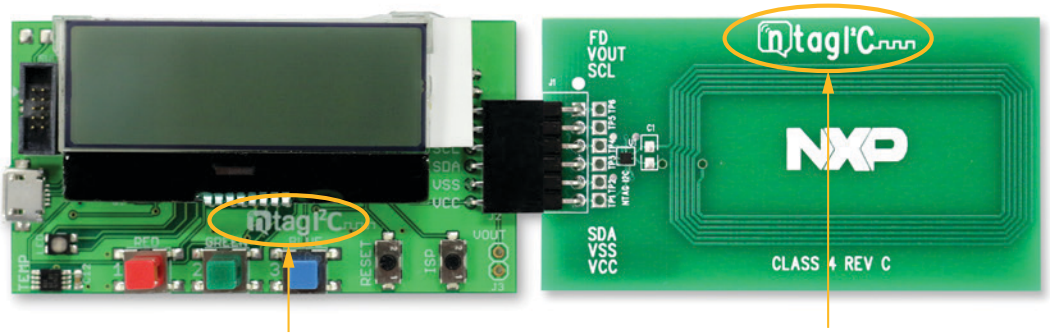

Figure 2-12. Explorer board to Antenna Board connection

Figure 2-13. Explorer Board with connected Antenna Board interacting with an NFC-enabled phone

Figure 2-14. NFC USB reader board to PC connection for firmware updates

Figure 2-15. NFC USB reader board in phone emulation mode interacting with the Explorer board/antenna board for demonstration purposes

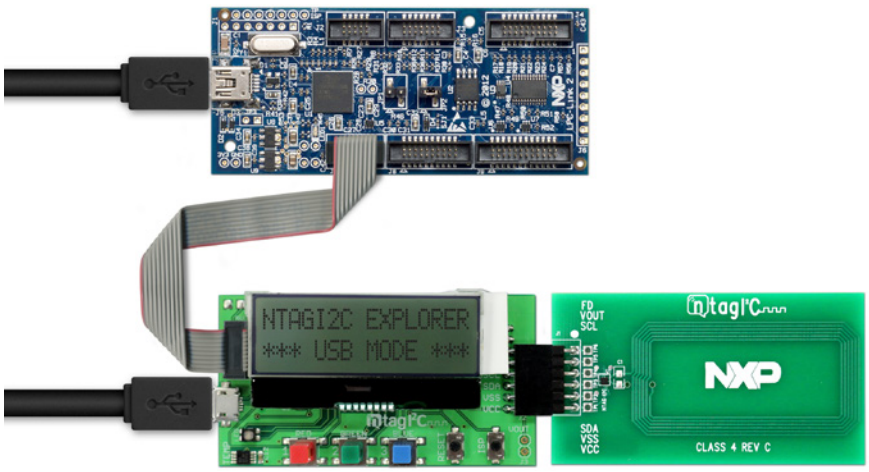

Figure 2-16. LPC-Link2 probe connected to Explorer board

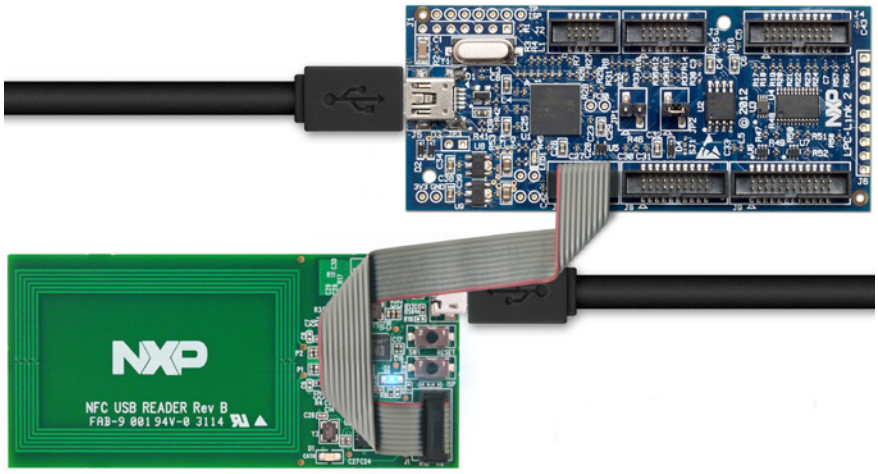

Figure 2-17. LPC-Link2 probe connected to NFC USB reader board

2.3.4 Enabling NFC on Android device

NFC data exchange must be enabled on your Android device in order for the demonstration kit to work. To enable NFC data exchange:

1. Navigate to the Settings application on your home screen.
2. Under Settings, select "More Settings"
3. Under "Wireless and Network," scroll down to the "NFC" option, and make sure this feature is turned on.

12:03
Wireless and networks
Network
Airplane mode
Mobile networks
Tethering and portable hotspot
Share your device's mobile data connection via USB, Wi-Fi, or Bluetooth
VPN
Set up and manage Virtual Private Networks (VPNs)
File/data transfer
NFC
Allow data exchange when device touches another device
S Beam
Ready to send file via NFC and Wi-Fi direct
Make sure NFC data exchange is enabled

Figure 2-18. Enabling NFC on mobile phone

2.3.5 Location of NFC antenna

The location of the NFC antenna varies from phone to phone. It's helpful both in using the tool and in debugging to know exactly where the location is for the phone you are using. For example in the Samsung Galaxy III phone, the NFC antenna is located in the battery. By lining up two sides of the battery with two sides of the NFC antenna traces, more successful NFC communication is possible (see Figure 2-19). For details about where to locate the NFC antenna for other phones, see Appendix A. Or alternatively, use the supplied RF detector (see Section 2.2.1.4) to find the strongest RF source location on your phone.

Figure 2-19. Best placement for successful NFC communication with Samsung Galaxy III mobile phone

2.3.6 NFC-enabled phone APK installation

In order to use your Android NFC-enabled phone as the demonstration GUI, you must download the NXP NTAG I²C Demoboard application from the Google Play Store:

1. Ensure that any previous versions have been uninstalled before initiating a new download.
2. Open the Google Play Store app.
3. Search for NXP I²C Demoboard.
4. Touch Install.
5. Touch Accept after reviewing the permissions.

You can also download the software over the Internet from http://nxp-rfid.com/ntag-i2c-explorerkit/

1. Ensure that any previous versions have been uninstalled before initiating a new download.
2. Navigate to the demonstration software download links in the Explorer page located at http://nxp-rfid.com/ntag-i2c-explorerkit/
3. Download ntagi2cdemoboard.apk
4. After downloading the .apk, locate it on your phone (e.g., under Settings/Storage/Downloads).
5. Select the NTAG I²C Explorer application and follow the directions for installing.

Note: Although you can set your phone to appear as a drive on a PC and copy .apk software to the appropriate location, and then eject your phone from the PC, you may not be able to locate the software on your phone using this approach even if you have loaded an application manager. If you encounter this problem, use one of the other two download approaches.

2.3.7 NTAG I²C Explorer board firmware load

The NTAG I²C Explorer kit comes with firmware loaded into the microprocessor. If newer versions are available, they will be accessible via the NTAG I²C Explorer-Board resources links at the bottom of the Explorer kit page located at http://nxp-rfid.com/ntag-i2c-explorerkit/

To load the firmware:

1. Locate your USB cable. Connect the micro-USB cable connector end to the Explorer board and the USB end to your PC.
2. Simultaneously hold down the RESET and ISP buttons on the Explorer board.
3. Release the RESET first.

4. Release the ISP second.
5. The Explorer board will now appear as a disk (named "CRP DISABLED") on your computer.
6. Click "Open the folder to view files" on the CRP DISABLED disk and delete the current "firmware.bin".
7. The new firmware image you are installing will be named " NTAG_I2C_Explorer_VXX.bin," where XX is the firmware revision. For example, if XX=20, then the firmware revision is 2.0.
8. Drag and copy the new file to the CRP DISABLED file directory.
9. Either eject the CRP DISABLED disk, or just unplug the USB cable from your computer.

Verify that the new firmware version has been loaded correctly by starting the NTAG I²C Demoboard application and placing the phone on the antenna. If operational, the board will harvest energy from the mobile device and "NTAGI2C Explorer" along with a second line indicating the temperature and voltage will display on the LCD screen (see Section 4).

Note: Typically, the Explorer board will not allow communication with the NFC-enabled mobile device if it is still connected via USB cable to the PC and there is any activity on the USB bus. In that case, users are expected to be utilizing the Peek and Poke functionality (see Section 4).

However, for phones which may have inadequate power to support power harvesting, there is an added feature, which allows the use of USB power for better coupling or for backlighting. In order to use this feature, press the blue button on the Explorer board, then connect the Explorer board to the PC using the micro USB to USB cable. To resume using the Peek and Poke functionality, disconnect the USB cable from the PC and reconnect without depressing any buttons on the Explorer board.

2.3.8 NFC USB Reader board firmware load

The NFC USB Reader board comes with firmware loaded into the microprocessor. If newer versions are available, they will be accessible via the NTAG I²C Reader-Board resources links at the bottom of the Explorer kit page located at http://nxp-rfid.com/ntag-i2c-explorerkit/

To load the firmware:

1. Locate your USB cable. Connect the micro-USB cable connector end to the Reader board and the USB end to your PC
2. Simultaneously hold down the SW1 (RESET) and SW2 (ISP) buttons on the NFC Reader board (see Figure 2-7).
3. Release the RESET first.
4. Release the ISP second.
5. The Reader board will now appear as a disk (named "CRP DISABLED") on your computer.
6. Click "Open the folder to view files" on the CRP DISABLED disk and delete the current "firmware.bin".
7. Drag and copy the new file to the CRP DISABLED file directory.
8. Eject the CRP DISABLED disk or unplug the USB cable from the PC.
9. Reconnect the USB cable to the PC.

Verify that the new firmware version has been loaded correctly by starting the NTAG I²C Demo application and placing the Explorer Board antenna on the NFC USB Reader board antenna. If operational, the Explorer board will harvest energy from the mobile device and "NTAGI2C Explorer" along with a second line indicating the temperature and voltage will display on the LCD screen.

2.3.9 NTAG I²C PC demo GUI for PC software installation

In order for the NFC USB Reader to emulate the Android phone, you must download the NFC USB Reader GUI Software accessible via the NTAG I²C Reader-Board resources links at the bottom of the Explorer kit page located at http://nxp-rfid.com/ntag-i2c-explorerkit/

1. The NFC USB Reader board arrives loaded with firmware. When updates are available, they will be available for download from http://nxp-rfid.com/ntag-i2c-explorerkit/ (see Section 2.3.8)
2. Download the NFC USB Reader GUI Software Executables folder to a PC subdirectory of your choice.
3. Unzip it.
4. Locate the "NTAG_I²C_Demo.exe" file, and double click on it.
5. When properly launched, you should see a small window that emulates a mobile device screen.

2.3.10 Peek and Poke GUI software installation

The Peek and Poke software is a PC-based software tool, which developers can use to view the EEPROM/ SRAM contents in an NXP Semiconductors NTAG I²C tag chip. For hardware setup, see Section 2.3.3. For software operation, see Section 4.

To begin the software installation process:

1. Navigate to http://nxp-rfid.com/products/ntag/ntag-i2c-explorer-demonstration-and-development-kit/
2. Register in order to make links at bottom of page valid.
3. Locate the NTAG I²C Explorer Board Resource links column, and click on the "Peek and Poke GUI" link.

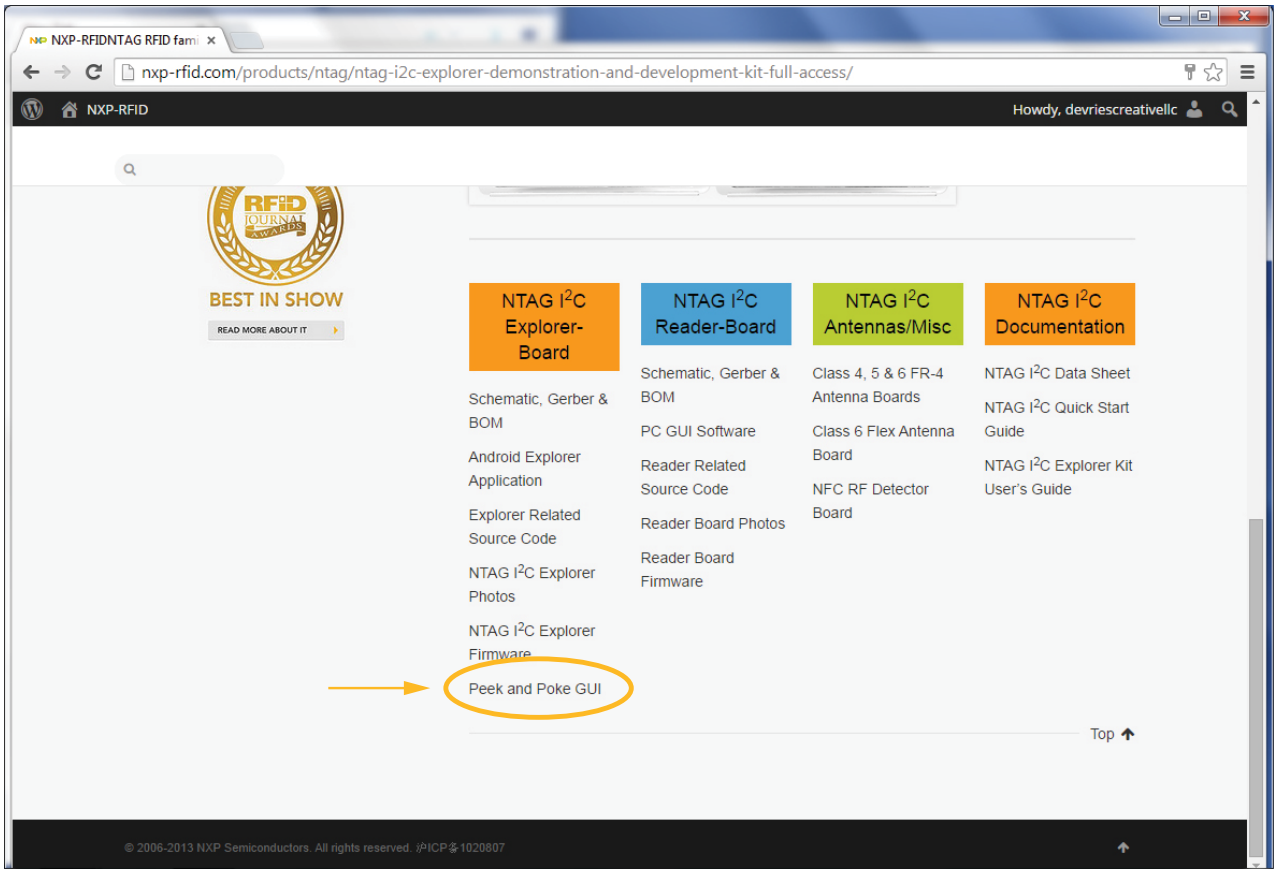

Figure 2-20. Explorer Kit resources links area

4. Download "NXP NTAG-I²C Explorer Software (Peek and Poke GUI).zip"
5. This file will contain the Peek and Poke GUI software, as well as some supporting files.
6. Double-click on the NTAG-I²C Explorer application file, which will result in dialog box suggesting you extract all files.

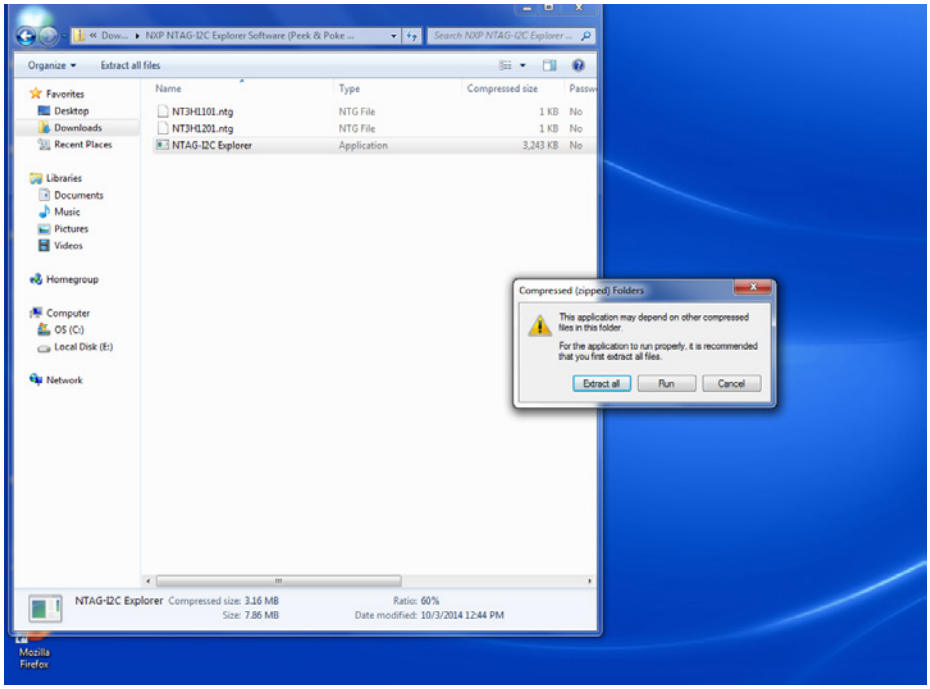
Compressed (zipped) Folders
This application may depend on other compressed files in this folder.
For the application to run properly, it is recommended that you first extract all files.
Extract all
Run
Cancel

Figure 2-21. Extract all Peek and Poke GUI files dialog box

7. Extract all files in a directory of your choice on your computer.

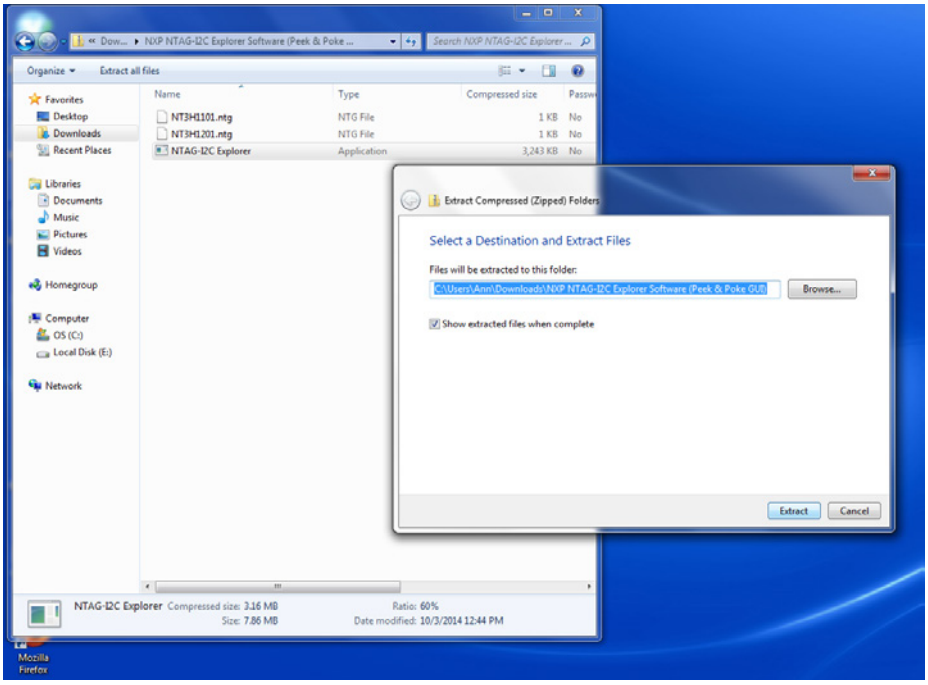

Figure 2-22. File Location dialog box for Peek and Poke GUI files

8. Double-click on the "NXP NTAG I²C Explorer" Application file, and click on "Run" when you encounter the security warning dialog box.

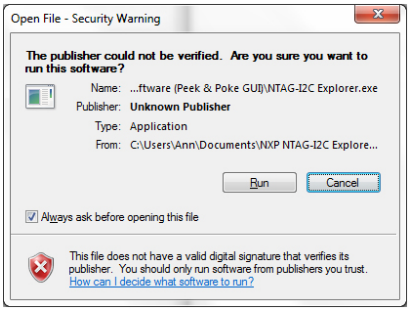
Open File - Security Warning
The publisher could not be verified. Are you sure you want to run this software?
Name: ...ftware (Peek & Poke GUI)\NTAG-I2C Explorer.exe
Publisher: Unknown Publisher
Type: Application
From: C:\Users\Ann\Documents\NXP NTAG-I2C Explore...
Run
Cancel
Always ask before opening this file
This file does not have a valid digital signature that verifies its publisher. You should only run software from publishers you trust.
How can I decide what software to run?

Figure 2-23. Security Warning dialog box

9. The program will begin and you should see the default screen. Unless you have already plugged in an Explorer board, the message along the footer will indicate "NTAG I²C Explorer hardware not detected".

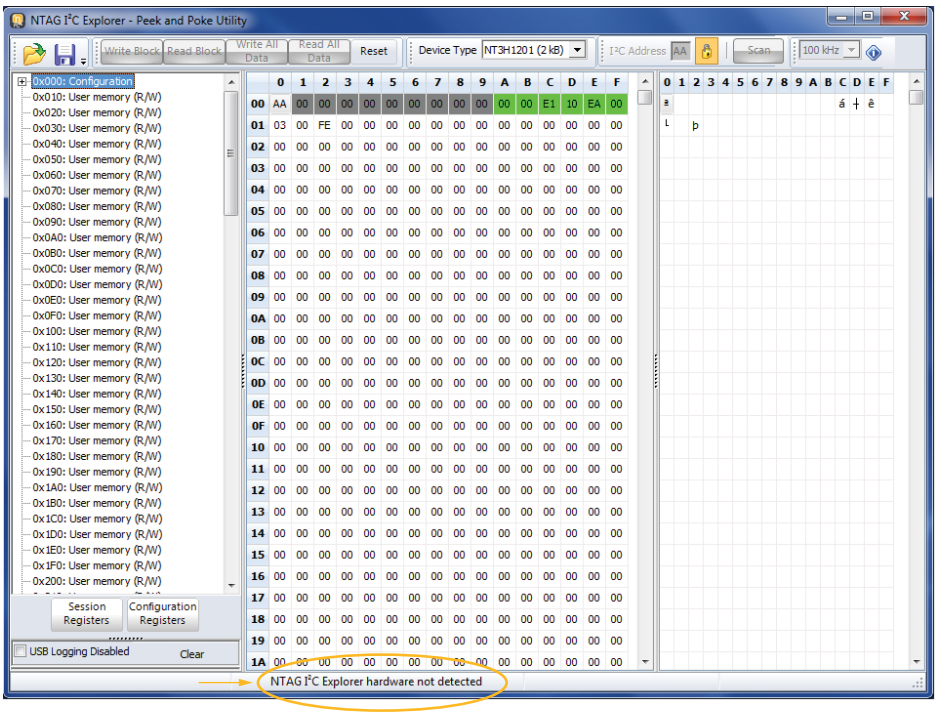

Figure 2-24. Peek and Poke GUI landing screen—No Hardware Detected

10. Using the supplied MicroUSB to USB connector, connect the Explorer board/NTAG I²C antenna board combination to your computer. After connecting the boards, the Explorer board LCD will display "NTAGI2C EXPLORER USB MODE" and the Peek and Poke GUI will indicate the "NTAG I²C Explorer hardware detected".

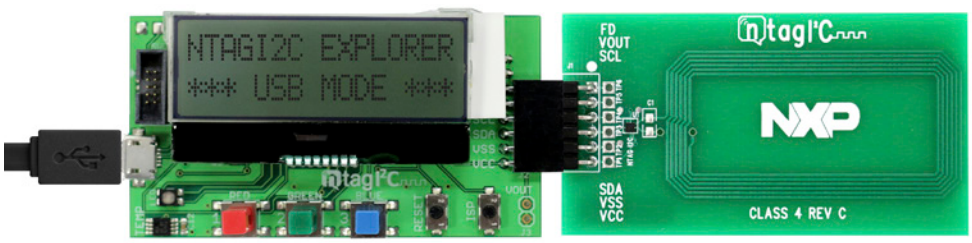

Figure 2-25. Explorer Board connected to an NTAG I²C antenna board in USB mode

3 NTAG I²C Demoboard Android phone application

The NTAG I²C Demoboard Android phone application turns an NFC-enabled mobile phone into an demonstration interface for the NTAG I²C tag chip capabilities. If an NFC-enabled phone is not available, use the NFC USB Reader to perform the same functions (see Section 5).

3.1 Splash window

The Splash window (see Figure 3-1) is the first activity to be displayed when the application is launched. This window will automatically close after 2 seconds.

Figure 3-1. Splash window

3.2 Default home screens and power harvesting

After the Splash window closes, the screen shown in Figure 3-2. will appear. This screen allows the user to launch the LED demo, NDEF demo, Speed Test Demo, and access the configuration functionalities supported by the application. Ensure that you have the latest copy of Explorer board firmware installed by touching the information circle at the upper right of the home screen. Note: because the board microprocessor shares the firmware version of the board with the application when performing the LED demonstration (see Section 3.3), this information will not be available to the application until the demonstration has executed at least once.

Note that the NTAG logo is grey, and "Choose option" is displayed. The explorer board LCD will be blank, and the LED will be dark. At this point, there is no power to the Explorer board.

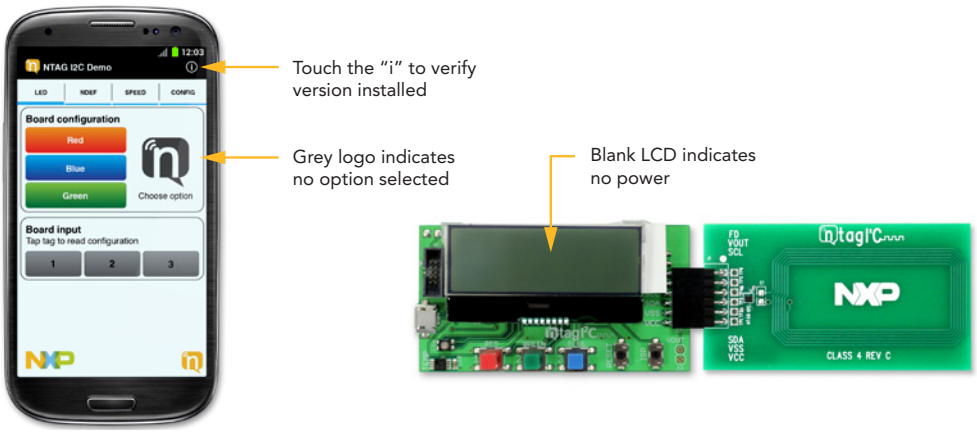

Figure 3-2. Default Explorer and mobile phone app home screens

Prior to beginning the demonstration, use the RFID detector board to ensure that you have NFC capability enabled on your phone, and that you've determined the optimal coupling location between your phone's antenna and the Explorer antenna board.

To begin the demonstration, lay your mobile device onto the antenna. If properly communicating and sound on your mobile device is turned on, you will hear a two-note tone indicating NFC communication. The NTAG device board will harvest power from the RF field and deliver it to the Explorer board to power up the microprocessor, which illuminates the LCD with the text "NTAGI2C Explorer" on the first line, and the harvested voltage and temperature readings on the second line (Figure 3-3).

Figure 3-3. Explorer board receiving power from NTAG I²C via power harvest function

3.3 LED tab

The LED Demo shows in an intuitive way the Energy harvesting and Pass-through mode features of the NTAG I²C device.

The Energy harvesting functionality allows the NTAG I²C tag chip to power up the microcontroller with energy obtained from the RF interface. Using this energy, the microcontroller executes its code and switches on the LEDs using zero external consumption as long as the NFC mobile device is in close proximity.

The Pass-through mode allows bidirectional communication between the NFC mobile device and the NTAG I²C Explorer board. On one side, the Android board configuration application transmits the user-selected color (red, blue or green) to the NTAG I²C Explorer microcontroller. On the other side, the NTAG I²C Explorer microcontroller transmits the voltage and temperature measured in its sensors and the identifiers of the buttons pressed (color and number) to the Android device. The Android application displays this information in the "Board Input" section of the LED tab screen.

3.3.1 Configuring board to demonstrate RF to I²C communication

The board configuration part of the demonstration shows how the NTAG I²C tag chip passes a command from the RF input through the I²C serial bus interface output to the microprocessor, which in turns acts upon the command, and lights the appropriate LED.

1. Lay your mobile device on the antenna. When properly placed, the two-note, NFC communication tone will sound, the LCD will display the NTAG I²C Explorer text, the harvested voltage, and it will also indicate the

temperature sensed by the board (in this case ambient). The mobile device displays the same information with one digit more resolution.

2. Touch one of the Board Configuration buttons (Red, Blue, or Green) on your mobile device under the LED tab on the home screen. The NTAG Icon will change color, indicating the color selection (Figure 3-4, Figure 3-5, and Figure 3-6), and the NTAG I²C Explorer board LED will illuminate in the chosen color.

Figure 3-4 Red LED board configuration selection

Figure 3-5 Blue LED board configuration selection

Figure 3-6. Green LED board configuration selection

3.3.2 Reading board input to demonstrate I²C to RF communication

The three colored and numbered buttons (Red/1, Green/2, and Blue/3) on the Explorer board demonstrate information from the board being transferred from the microprocessor through the I²C serial bus to the NTAG I²C tag chip, which then sends it via the RF field to the mobile device for display. When pressed, each colored and numbered

button on the Explorer board will cause a corresponding numbered box on the mobile device to display in the appropriate color.

Figure 3-7. Reading board input, red button

Figure 3-8. Reading board input, green button

Figure 3-9. Reading board input, blue button

3.3.3 Temperature sensor

The Explorer board displays ambient temperature unless one touches the temperature sensor. Hold a finger on the sensor and watch the temperature display immediately indicate the rising temperature over ambient. The temperature displays both in the LCD and also on the mobile device under "Board Input."

This operation demonstrates the NTAG I²C tag chip operating in pass through mode, where data passes through its SRAM. It is also another demonstration of passing data from the microprocessor through the I²C serial bus to the NTAG I²C tag chip, which in turn sends the data through the RF interface for display on the mobile device.

Figure 3-10. Temperature sensor demonstrates SRAM pass through mode

3.4 NDEF tab

The NDEF tab demonstrates reading and writing of NDEF content to the NTAG I²C tag chip.

3.4.1 Writing NDEF data

In the Write NDEF mode, the application allows the user to write a Text type, URI type, or Bluetooth pairing type NDEF message. URI-type NDEF messages allow NFC tags to trigger actions on an NFC device (usually a smartphone), such as opening a webpage or sending an SMS message. Bluetooth pairing NDEF messages contain information about a Bluetooth device that allow the smartphone to pair with that Bluetooth device by just tapping the tag. In the case of writing a Bluetooth pairing type message, it is important to remember that the MAC address shall be 6 bytes in hexadecimal (therefore, 12 characters from 0 to F).

To NDEF format the NTAG I²C tag chip, or write new data:

1. Remove the mobile device from the antenna.
2. Select "Write NDEF" from the tab on the right of the mobile device screen.
3. Type a message into the NDEF message area. Or alternatively, touch "Write default NDEF message," on your screen, which uses Text type as default and will enter the words "NTAG I²C EXPLORER" in the text window (see Figure 3-11).
4. Lay the mobile device onto the antenna.
5. When you hear the two-note tone indicating NFC communication, check the screen. A proper write will result in a message on the mobile device indicating, "write tag successfully done."

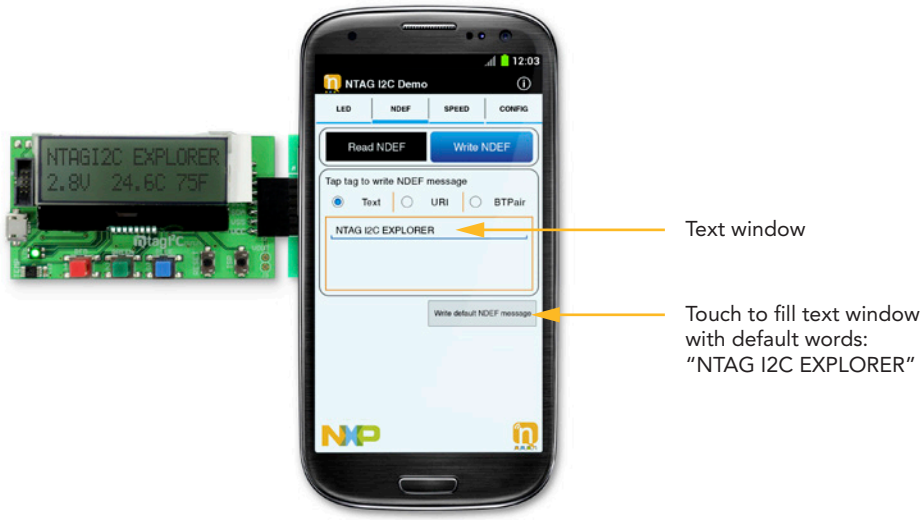

Figure 3-11. Default NDEF entry option

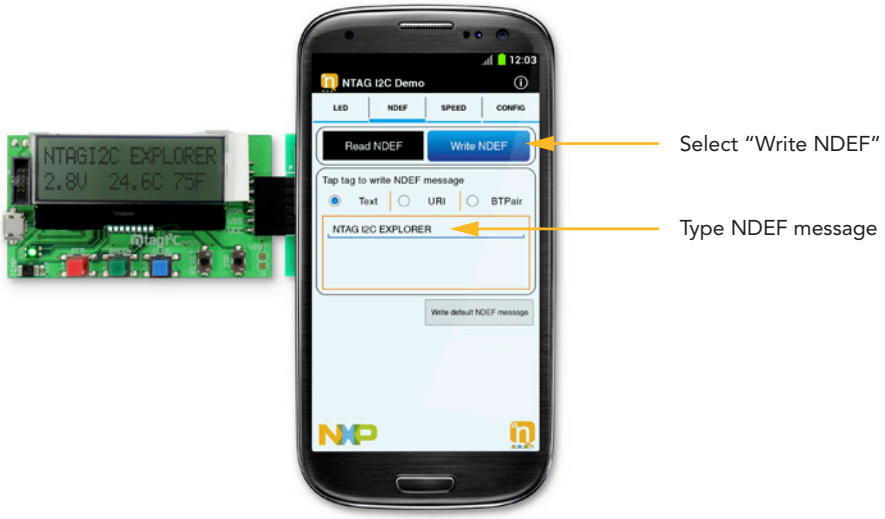

Figure 3-12. Writing NDEF data to NTAG I²C tag chip

3.4.2 Reading NDEF data

To read an NDEF formatted NTAG I²C tag chip:

1. Remove the mobile device from the antenna.
2. Select "Read NDEF" from the tab on the left of the mobile device screen.
3. Lay the mobile device onto the antenna.
4. When you hear the two-note tone indicating NFC communication, check the screen. A proper read will result in a message on the mobile device indicating, "read tag successfully done." See Figure 3-13. If the tag chip has not been NDEF formatted, placing the mobile device on the antenna will result in a message "NTAG I²C product is not NDEF formatted."

Figure 3-13. Reading NDEF formatted NTAG I²C tag chip

3.4.3 Displaying NDEF on the Explorer board LCD

You can also display the NDEF data on the Explorer board LCD. To do so:

1. Select the LED tab on your mobile device
2. Touch the "Display NDEF Message" selection box to enable LCD message display (see Figure 3-14).
3. Lay your mobile device on the antenna. The stored NDEF data will scroll through the LCD as long as the selection box has been checked.

Figure 3-14. Displaying NDEF on Explorer LCD

3.5 Speed tab

The Speed demonstration measures the transfer bit rate when communicating with the NFC Explorer board in different configurations.

3.5.1 SRAM board configuration

In SRAM configuration, the Android application operates in Pass-through mode for the transmission and reception of data when communicating with the NTAG I²C Explorer board. Data to be transmitted for the transfer bit rate calculation is the number of 64-byte blocks defined by the user in the block multiplier field (see Figure 3-15). This test indicates the performance of the communication in Pass-through mode from the application to the microcontroller, and from the microcontroller to the application.

Figure 3-15. Speed test SRAM configuration

The SRAM mode defines two methods for the data transfer: Fast Mode and Polling Mode. In Fast Mode the data is transmitted as soon as it is ready in the application, while in the polling mode the application checks to verify that the transferred data has been read by the Explorer board microcontroller (via information obtained from the Session Registers) before transferring a new block. It also checks if the Explorer microcontroller has written new information before reading the SRAM block. Therefore, the Fast Mode method will always return higher bit rates than the Polling Mode method.

The integrity of the data transferred in both directions is checked by appending a CRC32 value in the last block. The CRC32 is calculated for the whole message that has been transferred. If the CRC32 from the message received by the application is correct, the application will display an "Integrity of the data: OK" message. If the CRC32 from the message received by the board is correct, it will turn on the green LED at the end of the Speed Test.

3.5.2 EEPROM configuration

In the EEPROM configuration (see Figure 3-16), the Android application operates via the EEPROM memory, and thus, there is no communication with the NTAG I²C Explorer Board (Pass-through mode not used). The content is stored in the form of an NDEF text-type message, and the payload is calculated as the data present in the EEPROM field repeated as many times as the user indicates in the Block Multiplier field.

When the transmission completes successfully, the Android application displays the number of bytes, mean speed and time for both the reading and writing process measured for this particular communication. The user can also check the content of the memory to ensure that the NDEF message has been written appropriately.

Figure 3-16. Speed test EEPROM configuration

3.6 Config tab

The Config Tab allows the user to read tag memory, reset tag memory to its default, read session registers, and read from or write to configuration registers. For explanation of the tag memory configuration, reference the data sheet. For more information about the session and configuration registers, please see Sections 4.4.3 and 4.4.5.

Selecting the "Config" tab will bring up the landing screen shown in Figure 3-17. From this screen, the user may select to *Read Tag Memory*, *Reset Tag Memory*, *Read Session Registers*, or *Read/Write Config Registers*.

Figure 3-17. Config tab landing screen

3.6.1 Reading tag memory

To read the tag memory:

1. Select "Read Tag Memory" from the Config Tab Landing screen. A screen similar to that shown in Figure 3-18 will display.
2. Tap the mobile device to the tag antenna.
3. The two-note tone indicating NFC communication will sound and the screen will display the entire memory contents. See Figure 3-19. The user should tap the mobile device to the NTAG I²C tag chip for some time (about 2 to 3 seconds) to read the memory content.

Figure 3-18. Tap to read screen

Figure 3-19. Read tag memory selection results

3.6.2 Resetting tag memory

The reset function resets the memory of the NTAG I²C tag chip to the original content programmed in it during production (sets the fifth page of the EEPROM memory to a known value [the capability container] and the rest of the memory to zero):

1. Select "Reset Tag Memory" from the Config Tab Landing screen. A screen similar to that shown in Figure 3-18 will display.
2. Tap the mobile device to the tag antenna. The user should tap the NTAG I²C device for some time (about 2 to 3 seconds) to reset the memory content. A dialog is displayed on the screen as long as the operation goes on.
3. Upon successful reset, a banner indicating completion will display along the bottom of the screen (see Figure 3-20). If not successful, remove the mobile device from the antenna and try again.

Figure 3-20. Reset tag memory window

3.6.3 Reading session registers

Session registers are used to configure or monitor the register values of the current communication session. Session register values can be modified within a particular communication session. However, after Power-On Reset, these values return to the default configuration values.

Session register values can be read in Pages F8h to F9h (sector 3) via RF or block FEh via the I²C serial bus. However, they can only be written via the I²C serial bus.

For further information about the session registers' bytes please consult the NTAG I²C tag chip datasheet.
To read the tag session registers:

1. Select "Read Session Registers" from the Config Tab Landing screen. A screen similar to that shown in Figure 3-18 will display.
2. Tap the mobile device to the tag antenna.
3. Upon successful read, the screen similar to that shown in Figure 3-21A will display. Tapping on any of the right-facing arrows will bring up more details, as shown in Figure 3-21B. For on/off selections, a blue checkmark indicates "on" or selected (see Figure 3-21C).

Figure 3-21. Read session registers screen

Figure 3-22. Read configuration registers screen

3.6.4 Reading/writing configuration registers

To read the tag configuration registers:

1. Select "Read/Write Config Registers" from the Config Tab Landing screen. A screen similar to that shown in Figure 3-18 will display.
2. Tap the mobile device to the tag antenna.
3. Upon successful read, a screen similar to that shown in Figure 3-22 will display. Note the blue "Read Config" banner at the top of the screen. This indicates the active selection.
4. To write to the configuration registers, remove the mobile device from the antenna and touch "Write Config." The screen shown in Figure 3-23A will display. Register contents are controlled either via dropdown menus (Figure 3-23B), direct input (e.g., number pad, see Figure 3-23C) or by slider controls where grey indicates "off" and blue indicates "on" (Figure 3-23D).

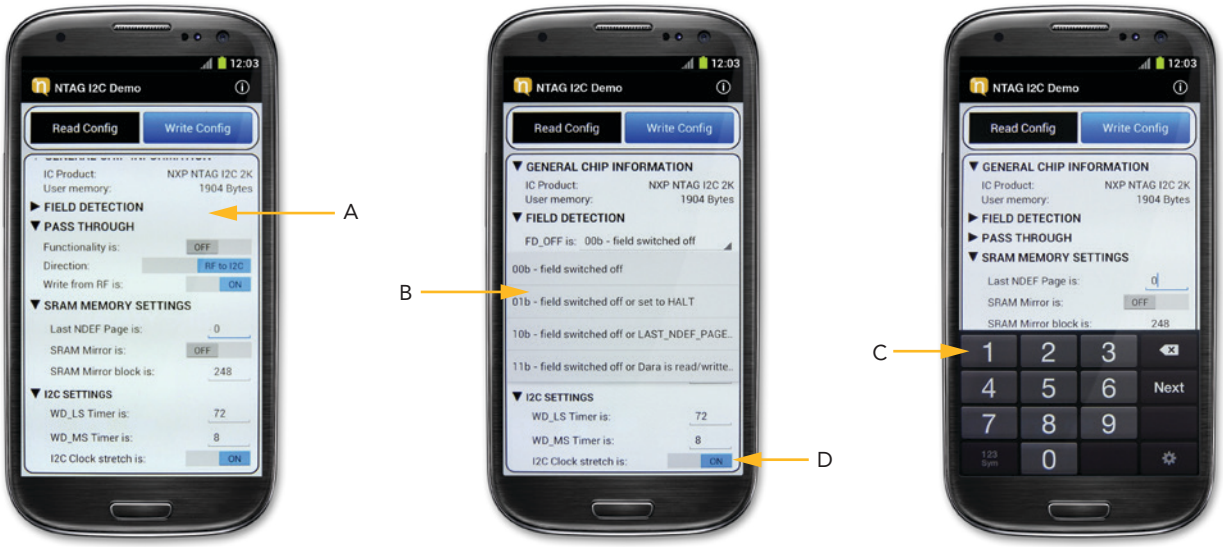

Figure 3-23. Write configuration registers

4 NTAG I²C Explorer Peek and Poke GUI

The Peek and Poke software is a PC-based software tool, which developers can use to view the EEPROM/ SRAM contents in an NXP Semiconductors NT3H1101 (1 Kbyte) or NT3H1201 (2 Kbyte) NTAG I²C tag chip. This software allows users to read from and write to the memory in the NTAG I²C tag chip via the I²C serial bus interface, as well as control the Session and Configuration registers.

Because developers can also read from or write to the NTAG I²C tag chip memory via the RF interface (for example, by using an NFC-enabled mobile phone), the tool supports bidirectional communication verification between the I²C serial bus and RF interfaces.

This capability is very useful for debug purposes when developing independent applications that must communicate through the NTAG I²C tag chip. For example, one use might be to verify correct operation of software running on a microcontroller embedded in a printed circuit board (I²C side), which must work in conjunction with software running on an independent NFC reader (RF side).

The USB hardware uses the HID class, so no additional drivers need to be installed to use the software, allowing plug-and-play functionality.

4.1 NTAG I²C Explorer Peek and Poke GUI overview

Upon software start up, the GUI shown in Figure 4-1 will display on the PC screen. The top bar (see Figure 4-1A) contains most of the GUI controls, which are described in the paragraphs below.

The left column lists the NTAG memory locations by hexadecimal address, with each line representing 16 bytes of data (for example, the highlighted row covers addresses from 0x2C0 through 0x2CF (see Figure 4-1B).

The center column displays the contents of those addresses in hexadecimal format, with one entry for each two bytes. The right column displays the ASCII representation of the data listed in the center column.

As an example, in Figure 4-1, the hexadecimal numbers 45 through 4A have been entered into the addresses corresponding to 0x2C9 though 0x2CE, respectively. Glancing at the right column, one can see that this represents the letters E through J. Location 0x2F has the hexadecimal value "61" entered (see Figure 4-1C), and it highlights in blue, as it is the currently active location. Note that the corresponding entry in the right column shows the ASCII character "a" (see Figure 4-1D), and highlights in grey. The bottom bar of the GUI also lists the active selected address (see Figure 4-1E).

The bar at the bottom of the GUI indicates presence or absence of any connected NTAG I²C hardware. In this case, the Explorer board is present and the software detects it, notifying the user with “NTAG I²C Explorer hardware detected” (see Figure 4-1F).

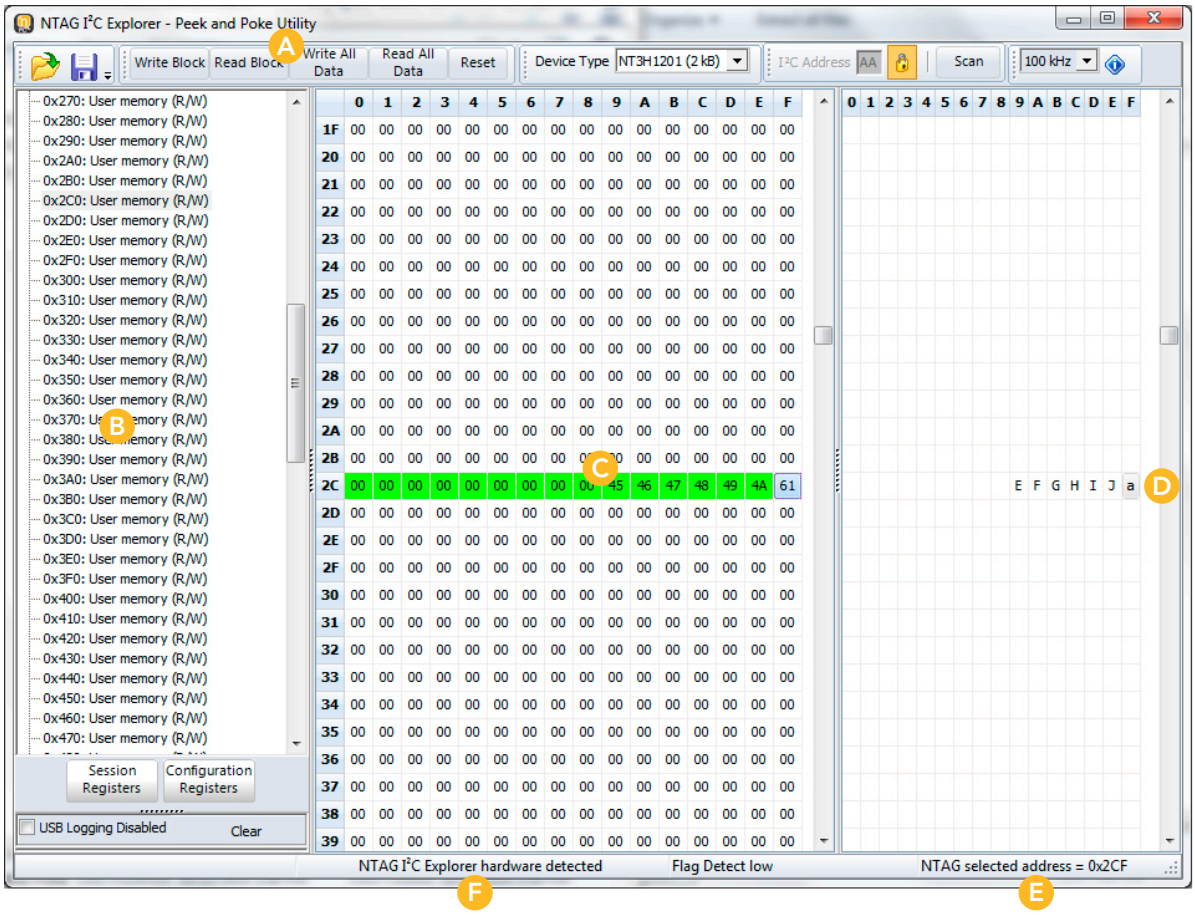

Figure 4-1. NTAG I²C Explorer initial screen

4.2 GUI top control bar details

4.2.1 Device type

The dropdown menu labeled "Device Type" indicates which version of the NTAG I²C chip has been detected. There are two versions of the NTAG I²C tag chip supported by the software (NT3H1101 and NT3H1201). The difference between the two devices is the amount of user memory available: the NT3H1101 contains 1 kB of user memory, while the NT3H1201 contains 2 kB of user memory. The software automatically detects which version of chip is connected by attempting to read location 07 Ah, which is the location of the configuration register accessible via the I²C interface in the 2 kB chip version. The configuration registers for the 1 kB version of the chip are located at block 03 Ah. (If you have a 2 kB version connected and attempt to switch the chip type to the 1 kB version, the software will alert you to the fact that it can read data at location 07 Ah and ask if you still want to switch chip types.)

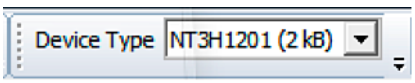

Figure 4-2. Device selection

4.2.2 Memory block selection

The memory in the NTAG I²C tag chip is configured in 16 byte data blocks. The software displays the memory block organization by hexadecimal address on the left side of the user interface. To examine the contents of a memory block, the user can click on that memory block in the left column.
For example, in Figure 4-3, the memory in block 0x000 contains the I²C Address, the serial number, Internal Data, Lock Bytes, and the Capability Container.

(With the exception of the I²C address, these names refer to the static memory structure required of an NFC Forum Type 2 Tag, such as the NTAG I²C tag chip. The I²C address is stored in a location reserved for internal data {bytes reserved by the specification for manufacturing use}. For more information about the required memory NFC tag chip format, visit nfc-forum.org, and download a specification.)

Clicking on an item in the left column (for example, the Capability Container in Figure 4-3) highlights the actual contents of the memory in the grid. The grid locations highlight in green if the memory is Read-Write (R/W), and in gray if it is Read-Only (R).

The software considers the highlighted 16-byte memory block to be the "active" block. In Figure 4-3, the active memory block is 0x000. The software uses the active block in conjunction with the Write Block or Read Block buttons (see Section 4.2.3 Read and write controls).

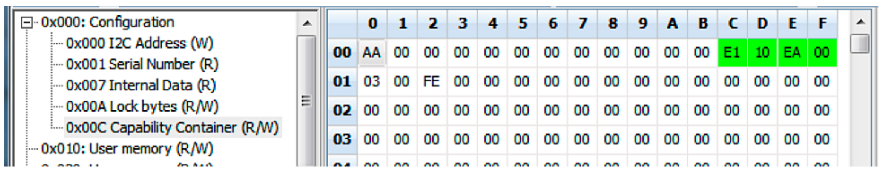

Figure 4-3. Memory block selection

4.2.3 Read and write controls

Figure 4-4 illustrates the buttons used to read from and write to the NTAG I²C tag chip via the USB-I²C interface. These buttons may be found at the top of the initial screen, as shown in Figure 4-1A.

- The Write Block button writes data input into the grid to the active 16-byte memory block (see the Memory Block Selection paragraph for the definition of an "active" block).
- The Read Block button reads from the 16-byte active memory block and displays it on the grid.
- The Write All Data button writes the contents of the grid to the NTAG I²C tag chip, except for the Session Register. The user can only edit the contents of the Session Register by pressing the Session Register button, or by selecting a cell in memory block 0xFE in the grid. When the Session register button is pressed, or when the user clicks in memory block 0xFE, the software will display the Session register dialog (shown in Figure 4-12).
- The Read All Data button reads the contents of the NTAG I²C tag chip, with the exception of the Session registers located in memory block 0xFE, and then displays the contents of the NTAG I²C tag chip memory in the grids.
- The Reset button loads the grids with the default contents of the NTAG I²C tag chip. It does not write the contents into the NTAG I²C tag chip memory. The Write All Data button must be used to load the Reset values into memory.

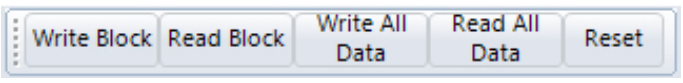

Figure 4-4. Read and write control buttons

4.2.4 Changing NTAG I²C tag chip memory contents

Change the contents of the NTAG I²C tag chip memory by entering hexadecimal values in the middle of the grid, or alternatively, by entering ASCii characters in the right side (see Figure 4-5). Changing the values in one side of the grid will automatically change those values in the other side.

Note: The software does not automatically send data to the NTAG I²C tag chip memory when the data in the grids change. The user must click the Write Block or Write All Data buttons to update the memory.

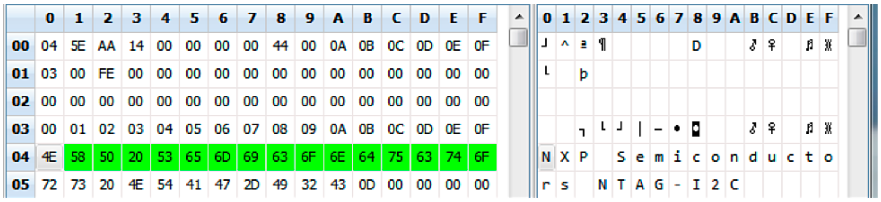

Figure 4-5. NTAG I²C tag chip memory display

4.2.5 I²C device address and scanning

The default I²C serial bus address of the NTAG I²C tag chip is 0xAA. The user can change the I²C serial bus address by writing to memory location 0x000. The software locks the value of the I²C serial bus address to 0xAA, unless it is unlocked by pressing the lock icon shown in Figure 4-6.

Note: The software does not use the value shown at memory location 0x000 in the data grid when programming block 0. The value in the edit box overrides the value in the grid. This approach ensures that the user does not accidentally change the value.

Figure 4-6. NTAG I²C tag chip address

To determine which I²C serial bus address has been programmed into the NTAG I²C tag chip, use the Scan button to find a device on the bus. After pressing the Scan button, the software will begin looking for an acknowledgement on the I²C serial bus. When it detects an acknowledgement, the scanning process will stop, and software will display the detected address as shown in Figure 4-7. Place this address in the I²C Address box, as shown in Figure 4-6.

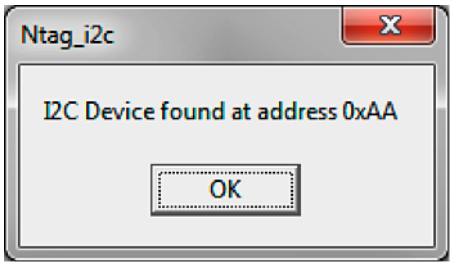

Figure 4-7. I²C serial bus address scanning

4.2.6 I²C clock frequency

Change the I²C serial bus clock frequency by selecting a data rate from the drop-down box, as shown in Figure 4-8. The maximum data rate supported by the NTAG I²C tag chip is 400 kHz.

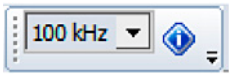

Figure 4-8. I²C serial bus clock selection

4.3 NTAG I²C Explorer lower left screen controls

4.3.1 USB data logging

To determine what data is actually being transmitted over the USB connection, select the "USB Logging Enabled" checkbox at the bottom left of the main GUI screen (see Figure 4-9A for the checkbox location).

Note: USB Data Logging does affect the amount of time required to Write All or Read All, so if speed is important, disable Logging.

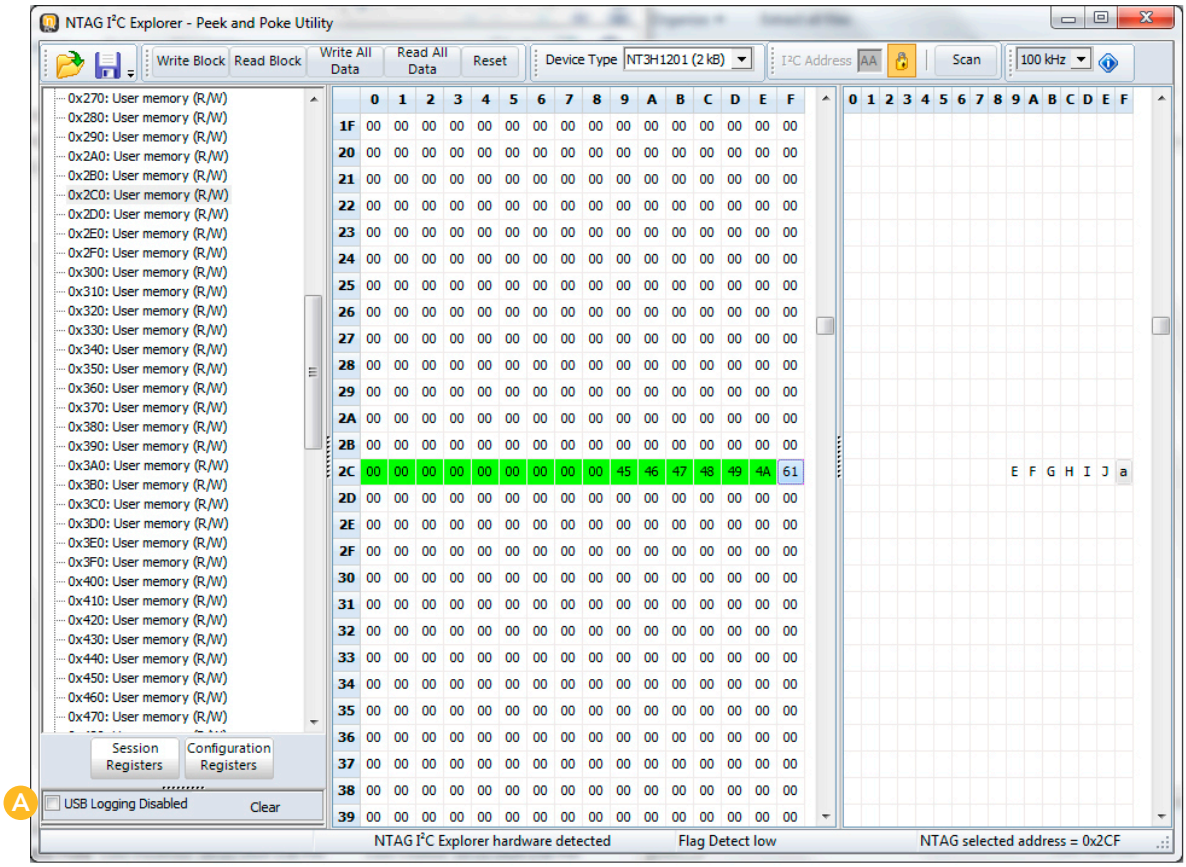

Figure 4-9. USB data logging control

When a read or write message transmits over USB, the contents of the message displays in the console below the checkbox (see Figure 4-10).

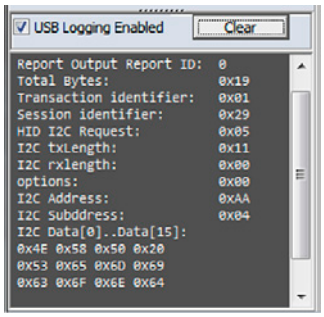

Figure 4-10. USB data logging

The USB HID message totals 65 bytes in length: 1 Report ID byte, and 64 data bytes. Although 65 bytes are sent/received in every USB transaction, the logging report only shows the data used by the USB-I²C hardware.
The following data is displayed:

- Total Bytes—the number of actual data bytes used for the message = 0x19 or 25d
- Transaction identifier—value is not critical and is not used
- Session identifier—value is not critical and is not used
- HID I²C Request—use 0x05, which is an I²C serial bus write/read request
- I²C txLength—number of data bytes to write to the I²C serial bus
- I²C rxLength—number of data bytes to read from the I²C serial bus
- Options—0x00. No special options required
- I²C Address—displays the I²C serial bus address of the NTAG I²C tag chip. Note that this is a 7-bit address with the read/write bit appended
- I²C Subaddress—displays the memory block address of the NTAG I²C tag chip
- I²C Data[0]..Data[15]—there are always 16 data bytes provided whenever data is sent to the NTAG I²C tag chip, except when programming the Session Register.

4.3.2 Session register

If the user clicks the Session Register address 0xFE, or the Session Registers button (see Figure 4-11), the GUI displays the Session Register details (see Figure 4-12).

Note: Individual bit definitions are listed most significant bit to least significant bit. A check in a box representing a single bit indicates that bit will be set to a "1" on a write, or a "1" has been read back from the register. No check in a box representing a single bit indicates that bit will be set to a "0" on a write, or a "0" has been read from the register. Unless otherwise noted, if the full 8 bits of a register are not used, the control populates lsb first (for example, I²C clock stretching, controlled by register 0xFE5, is enabled if the least significant bit of 0xFE5 has been set to "1").

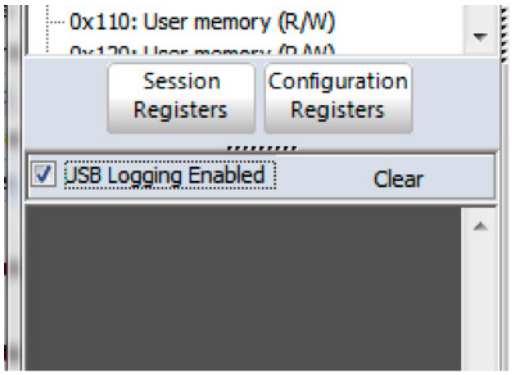

Figure 4-11. Session registers and configuration registers buttons

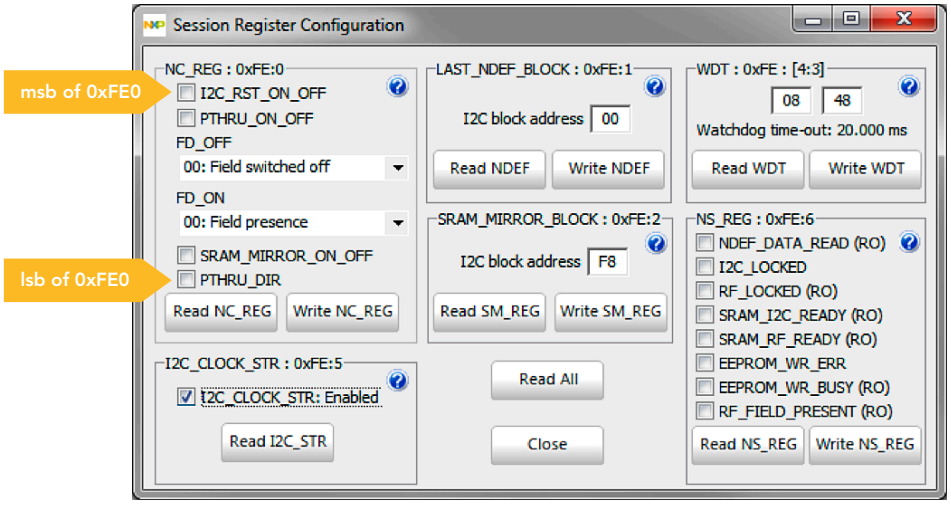

Figure 4-12. Session register

4.3.3 Session register details

Table 4-1 provides an explanation of the session register name abbreviations.

Table 4-1 Session register details

Register Name	Description
NC_REG: 0xFE:0	NTAG Configuration Register, located at block 0xFE, byte 0
I2C_RST_ON_OFF	When checked, enables soft reset through I²C repeated start (Used to allow combined read/write operations without releasing the bus and in this way guaranteeing that the data transfer is not interrupted. When this feature is enabled, if the microcontroller does not issue a STOP condition between two START conditions, this situation will trigger a reset of the I²C interface, and hence may hamper communication via the I²C interface. (Note that the NTAG Explorer software does not issue a STOP condition between two START conditions, so enabling this feature will automatically trigger a reset when the software attempts to communicate with the NTAG device.)
PTHRU_ON_OFF	When checked, enables the pass-through mode of the NTAG chip, where data passes from the RF interface through the SRAM to the I²C serial bus interface and vice versa, to avoid affecting the write cycle limitations of the NTAG EEPROM.

Register Name		Description
	FD_OFF	Pull-down menu used to select definition of when the Field Detect (FD) pin output stays high. ▸ 00b: in the event no RF field is present ▸ 01b: in the event no RF field is present, or the NTAG has been set to the HALT state ▸ 10b: in the event no RF field is present, or the last page of the NDEF message has been read (as defined in LAST_NDEF_BLOCK register) ▸ 11b: in the event no RF field is present, or if the last data has been read by the I²C interface (where pass through mode is in the RF --> I²C direction), or if the last data has been written by the I²C interface (where pass through mode is in the I²C --> RF direction).
	FD_ON	Pull-down menu used to select the event for which the Field Detect (FD) pin will be brought low. ▸ 00b: in the event an RF field is present ▸ 01b: in the event an RF field is present AND the first valid Start-of-Frame (SoF) has been received ▸ 10b: in the event an RF field is present AND the tag has been selected ▸ 11b: when in pass through mode in the RF interface --> I²C interface direction, and data is ready for reading at the I²C interface, OR when in pass through mode in the I²C interface --> RF interface direction, and data is read by the RF interface
	SRAM_MIRROR_ON_OFF	When checked, enables SRAM mirror mode
	PTHRU_DIR	Defines the data flow direction for pass through mode. If pass through has been enabled (PTHRU_ON_OFF=1) ▸ 0b: from the I²C interface --> the RF interface ▸ 1b: from the RF interface --> the I²C interface If pass through has not been enabled (PTHRU_ON_OFF=0) ▸ 0b: No write access from the RF side
LAST_NDEF_BLOCK: 0xFE:1		Allows input of the address for the last page of the NDEF message
SRAM_MIRROR_BLOCK: 0xFE:2		SRAM mirror lower page address in 4 page granularity ▸ 1h is page 4h (first page of User Memory) ▸ 2h is page 8h ▸ 3h is page Ch ▸ ... ▸ 74h is 1D0h
WDT: 0xFE:4 and OxFE:3		Watchdog Timer Because it is possible that the host can keep the I²C serial bus "locked" for a longer period, it is possible to program a watchdog timer to unlock the I²C host from the tag, so that the RF reader can access the tag. The host itself will not be notified of this event directly, but the NS_REG register (see Session Register descriptions) is updated accordingly (the register bit I2C_LOCKED will be cleared). The default value is set to 20 ms (848h), but the user can set the watchdog timer from 0001h (9.43 µs) up to FFFFh (617.995 ms). The timer starts ticking when the communication between the NTAG I²C and the I²C interface starts. If the communication with the I²C is still going on after the watchdog timer expires, the communication will continue until it completes. Then the status register I2C_LOCKED will be immediately cleared.
I2C_CLOCK_STR: 0xFE:5		When checked (lsb set to "1"), this register enables I²C clock stretching (see I²C serial bus specification for clock stretching details).
NS_REG: 0xFE:6		NTAG Session Register, located at block 0xFE, byte 6
	NDEF_DATA_READ	Indicates that all data bytes have been read from the address specified in LAST_NDEF_BLOCK
	I2C_LOCKED	Disables access to the configuration registers from the I²C serial bus interface
	RF_LOCKED	Disables access to the configuration registers from the RF interface
	SRAM_RF_READY	Indicates that data is ready in the SRAM for the RF interface to read
	SRAM_I2C_READY	Indicates that data is read in the SRAM for the I²C interface to read
	EEPROM_WR_ERR	HV voltage error during EPP cycle via I²C host
	EEPROM_WR_BUSY	Indicates whether or not the EEPROM is active ▸ 1b: EEPROM write cycle is active—access to the EEPROM is disabled ▸ 0b: access to EEPROM for write cycle is possible
	RF_FIELD_PRESENT	RF field is detected

4.3.4 Configuration registers

Edit the contents of the Configuration Registers (see Figure 4-13) by pressing the Configuration Registers button (refer to Figure 4-11) at the bottom left of the screen, or by clicking in the grid on memory block 0x3A for the NT3H1101 and 0x7A for the NT3H1201.

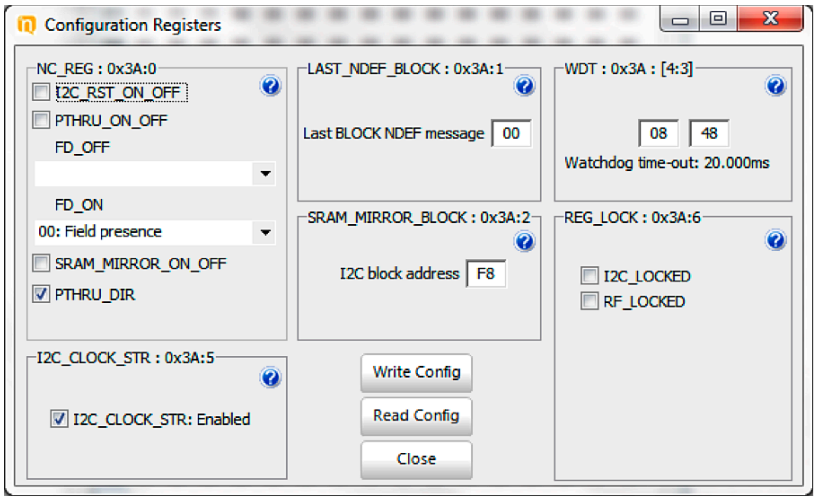

Figure 4-13. Configuration register

4.3.5 Configuration register details

Table 4-2 provides a more detailed explanation of the configuration registers.

Table 4-2 Configuration register details

Register Name	Description
NC_REG: 0x3A:0 or 0x7A:0	NTAG Configuration Register, located at 0x3A:0 for the NT3H1101 and 0x7A:0 for the NT3H1201.
I2C_RST_ON_OFF	When checked, enables soft reset through I²C repeated start (Used to allow combined read/write operations without releasing the bus and in this way guaranteeing that the data transfer is not interrupted. When this feature is enabled, if the microcontroller does not issue a STOP condition between two START conditions, this situation will trigger a reset of the I²C interface, and hence may hamper communication via the I²C interface. (Note that the NTAG Explorer software does not issue a STOP condition between two START conditions, so enabling this feature will automatically trigger a reset when the software attempts to communicate with the NTAG device.)
PTHRU_ON_OFF	When checked, enables the pass through mode of the NTAG chip, where data passes from the RF interface through the SRAM to the I²C serial bus interface and vice versa, to avoid affecting the write cycle limitations of the NTAG EEPROM.
FD_OFF	Pull down menu to select definition of when the Field Detect pin output stays high. ▸ 00b: in the event no RF field is present ▸ 01b: in the event no RF field is present, or the NTAG has been set to the HALT state ▸ 10b: in the event no RF field is present, or the last page of the NDEF message has been read (as defined in LAST_NDEF_BLOCK register) ▸ 11b: in the event no RF field is present, or if the last data has been read by the I²C interface (where pass through mode is in the RF --> I²C direction), or if the last data has been written by the I²C interface (where pass through mode is in the I²C --> RF direction).
FD_ON	Pull down menu to select event for which the Field Detect pin will be brought low. ▸ 00b: in the event an RF field is present ▸ 01b: in the event an RF field is present AND the first valid Start-of-Frame (SoF) has been received ▸ 10b: in the event an RF field is present AND the tag has been selected ▸ 11b: when in pass through mode in the RF interface --> I²C interface direction, and data is ready for reading at the I²C interface, OR when in pass through mode in the I²C interface --> RF interface direction, and data is read by the RF interface

Register Name		Description
	SRAM_MIRROR_ON_OFF	When checked, enables SRAM mirror mode
	PTHRU_DIR	Defines the data flow direction for pass through mode. If pass through has been enabled (PTHRU_ON_OFF=1) ▸ 0b: from the I²C interface --> the RF interface ▸ 1b: from the RF interface --> the I²C interface If pass through has not been enabled (PTHRU_ON_OFF=0) ▸ 0b: No write access from the RF side
LAST_NDEF_BLOCK: 0x3A:1 or 0x7A:1		Allows input of the address for the last page of the NDEF message
SRAM_MIRROR_BLOCK: 0x3A:2 or 0x7A:2		SRAM mirror lower page address in 4 page granularity ▸ 1h is page 4h (first page of User Memory) ▸ 2h is page 8h ▸ 3h is page Ch ▸ ... ▸ 74h is 1D0h
WDT: 0x3A:4/0x3A:3 or 0x7A:4/0x7A:3		Watchdog Timer Because it is possible that the host can keep the I²C serial bus "locked" for a longer period, it is possible to program a watchdog timer to unlock the I²C host from the tag, so that the RF reader can access the tag. The host itself will not be notified of this event directly, but the NS_REG register (see Session Register descriptions) is updated accordingly (the register bit I2C_LOCKED will be cleared). The default value is set to 20 ms (848h), but the user can set the watchdog timer from 0001h (9.43 µs) up to FFFFh (617.995 ms). The timer starts ticking when the communication between the NTAG I²C and the I²C interface starts. If the communication with the I²C is still going on after the watchdog timer expires, the communication will continue until it completes. Then the status register I2C_LOCKED will be immediately cleared.
I2C_CLOCK_STR: 0x3A:5 or 0x7A:5		When checked (lsb set to "1"), this register enables I²C clock stretching (see I²C serial bus specification for clock stretching details).
REG_LOCK: 0x3A:6 or 0x7A:6		
	I2C_LOCKED	Disables access to the configuration registers from the I²C serial bus interface
	RF_LOCKED	Disables access to the configuration registers from the RF interface

4.3.6 Help screens for session and configuration registers

For quick explanations for any of the registers listed under the session and configuration register screens, click on the small blue question mark (see Figure 4-14A). This action will bring up a help screen describing the register in a bit more detail (see Figure 4-14B).

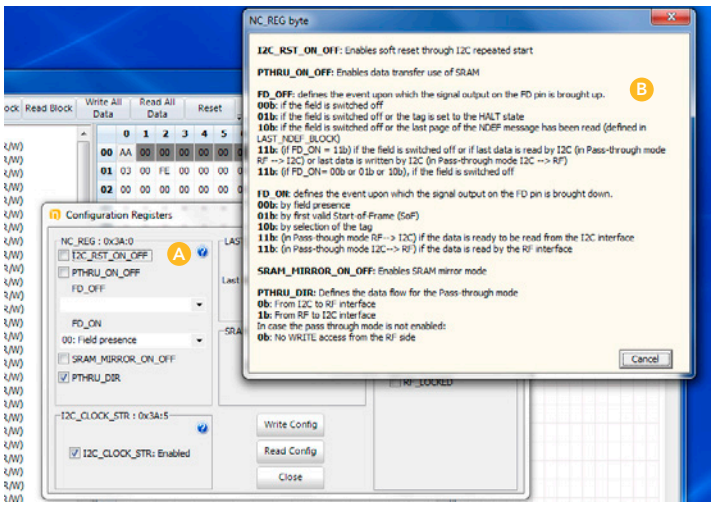
NC_REG byte
I2C_RST_ON_OFF: Enables soft reset through I2C repeated start
PTHRU_ON_OFF: Enables data transfer use of SRAM
FD_OFF: defines the event upon which the signal output on the FD pin is brought up.
00b: if the field is switched off
01b: if the field is switched off or the tag is set to the HALT state
10b: if the field is switched off or the last page of the NDEF message has been read (defined in LAST_NDEF_BLOCK)
11b: (if FD_ON = 11b) if the field is switched off or if last data is read by I2C (in Pass-through mode RF --> I2C) or last data is written by I2C (in Pass-through mode I2C --> RF)
11b: (if FD_ON= 00b or 01b or 10b), if the field is switched off
FD_ON: defines the event upon which the signal output on the FD pin is brought down.
00b: by field presence
01b: by first valid Start-of-Frame (SoF)
10b: by selection of the tag
11b: (in Pass-though mode RF--> I2C) if the data is ready to be read from the I2C interface
11b: (in Pass-though mode I2C--> RF) if the data is read by the RF interface
SRAM_MIRROR_ON_OFF: Enables SRAM mirror mode
PTHRU_DIR: Defines the data flow for the Pass-through mode
0b: From I2C to RF interface
1b: From RF to I2C interface
In case the pass through mode is not enabled:
0b: No WRITE access from the RF side
Cancel
Configuration Registers
NC_REG : 0x3A:0
I2C_RST_ON_OFF
PTHRU_ON_OFF
FD_OFF
FD_ON
00: Field presence
SRAM_MIRROR_ON_OFF
PTHRU_DIR
I2C_CLOCK_STR : 0x3A:5
I2C_CLOCK_STR: Enabled
Write Config
Read Config
Close
A
B

Figure 4-14. Session and configuration register help screens

5 USB NFC Reader

Use the USB NFC Reader when an NFC-enabled mobile device is not available, or when you require more power than a mobile device can provide. To start the demo:

1. Ensure that you've loaded all of the latest firmware and software required (see Sections 2.3.7 through 2.3.10).
2. Connect the Reader board to the PC using the USB cable.
3. Navigate to where you have installed the PC GUI software "NTAG_I²C_Demo" and double click on it.
4. A window emulating an Android device screen should appear on your monitor (see Figure 5-1).

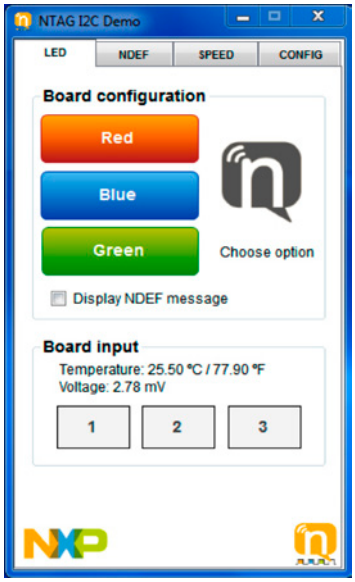

Figure 5-1. NFC USB reader gui start up screen

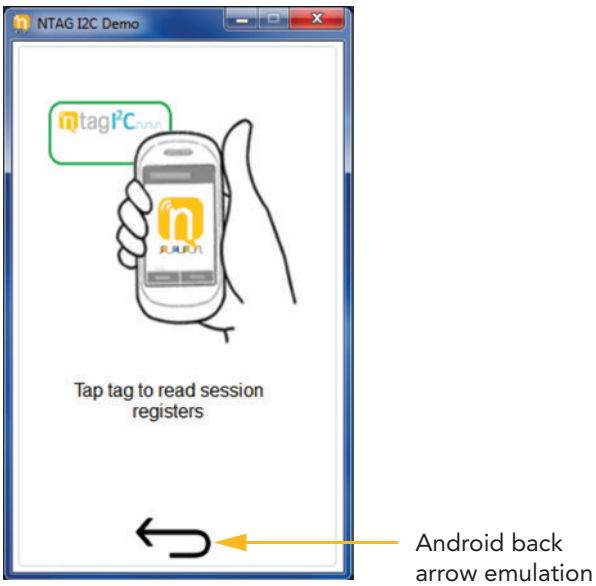

Figure 5-2. "Tap" screen with browser back arrow

After launching your NTAG_I²C_Demo GUI, the operation is almost identical to that of the Android application discussed in Section 3. The GUI will indicate when to "tap" the reader to the Explorer board (see Figure 5-2). In reality, you can just pick up the Explorer board/Antenna pair and lay it back down so that the Explorer antenna lies over the Reader board antenna. Note also the back arrow on the GUI that emulates the same function on an Android mobile device.

Note: Sometimes the demo GUI application fails to detect the reader and indicates 'No Reader Found' when launched. Close down the application, unplug the USB cable from the PC and reinsert it. Then relaunch the demo GUI.

6 LPC-Link2 debug probe

To enable fast development, the Explorer kit comes equipped with a LPC-Link2 debug probe. The LPC-Link2 probe ships pre-programmed with an CMSIS-DAP compliant debug image that allows a developer to utilize IDEs, such as the LPCXpresso, Keil MDK, and IAR EWARM.

Connect the USB connector (J5) to the probe, and using the provided 10-pin ribbon cable, connect J7 to the JTAG/SWD header on the LPC11U14 Explorer board. After making the connection, launch your preferred IDE and begin coding.

For more information about the LPC-Link2 debug probe, visit www.lpcware.com/lpcxpresso, where you can find help forums, downloads, FAQs, and more.

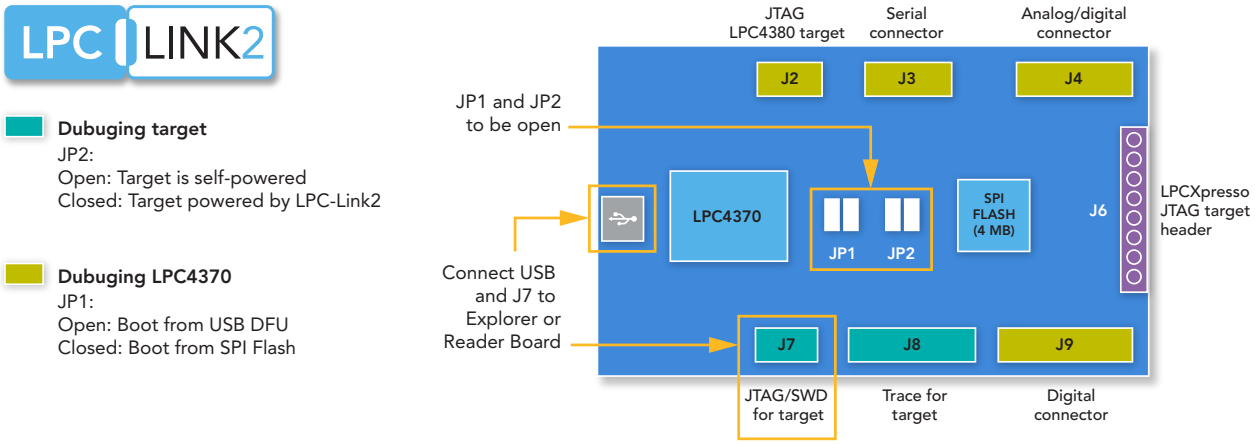

Figure 6-1. LPC-Link2 debug board (connect micro USB and J7 to Explorer or Reader Board — JP1 and JP2 to be open)

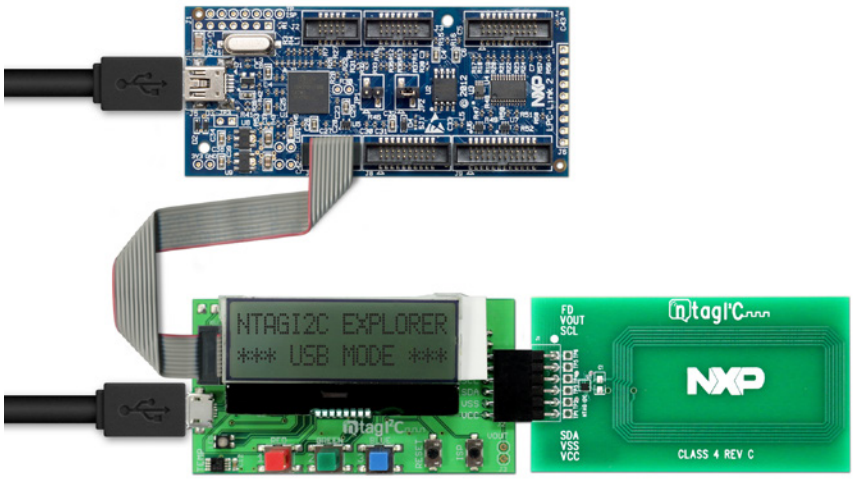

Figure 6-2. LPC-Link2 debug board connected to the Explorer Board

7 Summary

The NTAG I²C Explorer demonstration kit facilitates understanding of the many features of the NXP NTAG I²C tag chip and its potential for application in a wide variety of products. With the purchase of the optional LPC Link2 debug board, the demonstration kit additionally provides a development platform for application designers.

8 Appendix A: Optimal NFC phone placement

It sometimes takes a bit of experimentation to determine the optimal coupling between an NFC-enabled phone antenna, and one of the NTAG I²C antenna boards. For this reason, NXP has included an NFC RF detector board (NFC antenna with an LED indicator light) with the NTAG I²C Explorer Kit. This board is useful in determining whether or not a phone is NFC-enabled, and if so, where is the optimal placement of an external NFC antenna in order to achieve the best RF communication.

8.1 Using the NFC RF Detector Board

1. If you are not certain that you have an NFC-enabled phone, lay the phone on the NFC RF detector board and move it around. If the LED lights up, then the phone is NFC-enabled. Depending on the phone type, antenna sizes and placement differ, so you may need to experiment with, and adjust the placement of the phone versus the NFC RF detector board in order to find the optimal position.

   Note: in some cases, as in the Samsung phones, NFC antennas are located inside the battery case. If your phone battery has been replaced with an after market version, you may no longer have NFC capability. Look for the words, "Near Field Communication" under the Samsung logo to make sure you have an NFC-enabled phone.

Figure 8-1. Some NFC antennas are located inside the battery case as indicated by the words: "Near Field Communication".

2. The NFC RF Detector board has a similar LED-to-antenna orientation as the NTAG I²C board does between the NTAG I²C tag chip and the antenna. After you have ascertained that your phone is NFC-enabled and determined the position of optimal reception, make a note of where on the phone GUI display the LED lines up. Because the NTAG I²C chip is also centered on the PCB, chances are, the NTAG I²C antenna board will work best in a similar location.

   See examples for the popular Moto X and Samsung GII phones in Figure 8-2 and Figure 8-3, respectively, where the LED lines up near the words "Board input" on the GUI display, and the optimal NTAG I²C antenna board placement is in a similar location.

Figure 8-2. MotoX optimal antenna coupling location

Figure 8-3. Samsung Galaxy III optimal antenna coupling location

8.2 Selecting an NTAG I²C antenna board

Matching an NTAG I²C antenna to the form factor of an NFC-enabled phone antenna helps in obtaining the optimal coupling for the best communication. To illustrate, let’s examine both an easy case, and a more difficult one.

The easier case: Samsung Galaxy 5

The Samsung Galaxy 5 has a large antenna located in the battery pack. The orange shape shown in Figure 8-4 illustrates the approximate antenna form factor. The best coupling results when using a similarly sized NTAG I²C antenna, which in this case would be the Class 4 version. If using a Class 4 antenna is not feasible, try to line up at least two sides of the antenna when using the Class 5 or Class 6 options (see Figure 8-4, where the green shape indicates a Class 5 antenna form factor.

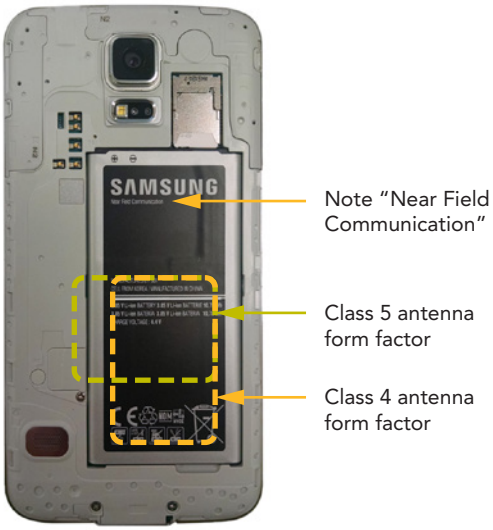

Figure 8-4. Samsung Galaxy 5 antenna location (back cover removed)

Figure 8-5 shows use of the NFC RF detector board as described in “Using the NFC RF Detector Board,” step 2 to locate the best point of coupling for the Samsung Galaxy 5, where one makes a note of how the LED lines up with the phone display and begins with the same orientation when using the NTAG I²C board.

Figure 8-5. Samsung Galaxy 5 optimal coupling antenna location

The more difficult case: HTC

The HTC phone antenna is harder to couple to for three reasons: its small size, its location surrounding the camera lens, and because it is behind metal (see Figure 8-6, where the orange shape indicates the antenna form factor). In this case, using the smaller NTAG I²C Class 6 antenna (see Figure 8-7), which approximates the shape of the HTC phone’s antenna, results in the best coupling and communication.

If you would like to experiment, try using the NTAG I²C Class 4 antenna board, and note the more inefficient coupling this selection provides.

Figure 8-6. HTC NFC antenna location

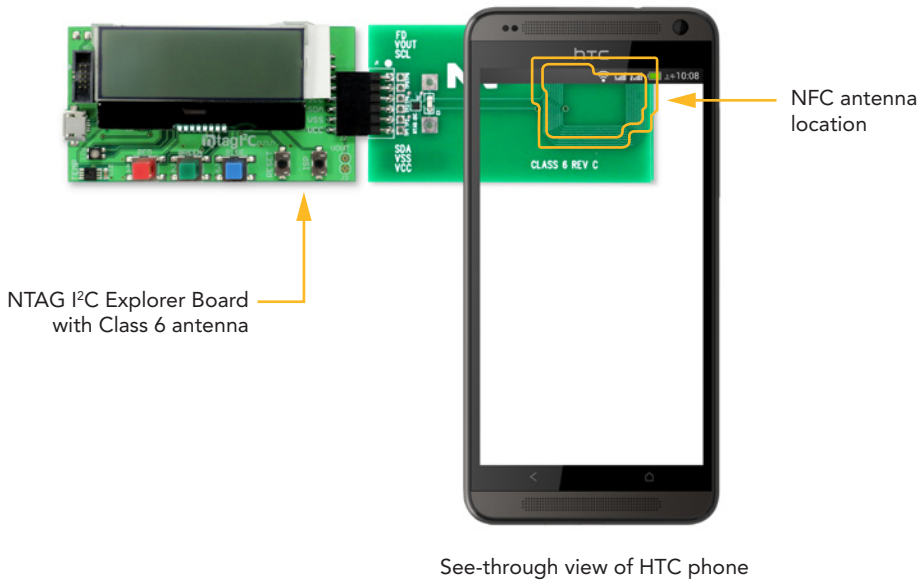

Figure 8-7. NTAG I²C Class 6 antenna coupled to an HTC phone

9 Appendix B: Application processing details

9.1 LED application

As the LEDs, display, and GUI require updating, the process performs iteratively, several times in a second. At each iteration:

1. The application writes the appropriate information into the SRAM of the NTAG. It writes which LED color should be shown:

Table 9-1

Byte	Value	Indicates
61	0x01	red color
	0x02	blue color
	0x03	green color
55	0	NDEF NOT displayed
	1	NDEF displayed

2. The microcontroller reads the SRAM, updating the LEDs and displays accordingly.
3. For buttons pressed on the Explorer board, the microcontroller writes the corresponding content to the SRAM:

Table 9-2

Byte	Value	Indicates
62	lsb	red button pushed
	second lsb	green button pushed
	third lsb	blue button pushed
58:59	temperature value	temperature at sensor
56:57	voltage value	voltage at sensor
63	firmware version value	Firmware version of Explorer board

4. Finally, the application reads that information and updates the GUI.

The application also sends back the temperature and voltage previously received from the board, because the computing power of a smartphone or PC is much higher than that of the Explorer board microprocessor. Therefore, the board sends directly the values obtained from the voltage and temperature sensors to the application, and the application calculates the actual values of the temperature and voltage and sends them back in ASCII to the board. This way, it sends back the temperature in Celsius in bytes 40 to 43, the temperature in Fahrenheit in bytes 45 to 49, and the voltage in bytes 56 and 57.

9.2 Speed test process

9.2.1 SRAM

The Speed Test begins as soon as the user taps the NTAG I²C tag antenna. At this point, the application writes a message in the SRAM indicating to the microcontroller that it will start the SRAM Speed Test, and waits until the microcontroller indicates that is ready (through the session registers of the NTAG I²C). The application then begins to write 64-byte blocks (with all bytes set to zero) to the SRAM memory, as many times as indicated by the user. After each time it writes to the SRAM, it recalculates the CRC32 with the new data sent, and if the Polling Mode is

active, it waits until the microcontroller has finished reading the SRAM. At the end, in the last block, the application sends a message indicating that it is the last one, and it also sends the CRC32 calculated in the last 4 bytes. The microcontroller checks the integrity of the data by comparing the CRC32 received with the one calculated from the data received.

Once this first phase has finished, the microcontroller begins writing 64-byte blocks (all zeros, again) to the SRAM. In Polling Mode, the application waits for the microcontroller to finish writing, while in Fast Mode it reads as fast as it can. In the last block the microcontroller sends the CRC32 calculated in the last four bytes. The application checks the integrity of the data by comparing this CRC32 with the one calculated from the data received.

Once the test has finished, both the application and the microcontroller indicate whether the integrity check was successful (through a green LED at the microcontroller), and the application shows the time, mean speed and data transferred for both directions.

9.2.2 EEPROM

The application creates the NDEF message to be written by creating a string that contains the content from the textbox as many times as indicated, and adding the appropriate header. The application then writes the created NDEF message to the EEPROM memory by sending as many NFC Forum standard type-2-tag Write commands as necessary, and measuring the time it takes to do so. Once it has finished writing, it reads the NDEF message by sending as many NFC Forum type-2-tag Read commands as necessary. Here it is important to note that, because the Write command writes bytes 4-by-4, and the Read command reads 16-by-16, usually the read bytes are more than the written bytes (see "NFC Forum Type 2 Tag Operation Specification").

10 References

10.1 General Reference Information and Resources

- http://nxp-rfid.com/ntag-i2c-design-resources/

10.2 Explorer Kit Resources

- http://nxp-rfid.com/ntag-i2c-explorerkit/

10.3 NDEF

In order to understand more about the different types of NDEF messages and their structures, please refer to the following NFC Forum specifications:

- "NFC Data Exchange Format (NDEF) Technical Specifications"
- "NFC Record Type Definition (RTD) Technical Specification"
- "NFC Text RTD Technical Specification"
- "NFC URI RTD Technical Specification"
- "NFC Forum Connection Handover Technical Specification"
- "Bluetooth Secure Simple Pairing Using NFC"

These specifications can be found by visiting:

- http://nfc-forum.org/our-work/specifications-and-application-documents/specifications/nfc-forum-technical-specifications/
- http://nfc-forum.org/our-work/specifications-and-application-documents/application-documents/

10.4 I²C Serial Bus Specification

To understand more about the I²C serial bus protocol, please see:

- I²C Serial Bus and User Manual Application Note from NXP: http://www.nxp.com/documents/user_manual/UM10204.pdf

10.5 Microcontrollers

To learn more about the Explorer kit's microcontrollers, and their use as a development tool, please visit:

- LPCXpresso development tool platform: www.nxp.com/lpcxpresso
- Software and support for NXP MCUs: http://www.lpcware.com
- LPC-Link2 debug probe: http://www.lpcware.com/lpclink2

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Date of release: November 2014

Published in the USA